3. Bipolar Junction Transistors

3.1 Transistor Construction

Transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layer of material or two *p*- and one *n*-type layers of material. The former is called *npn* transistor, while latter is called an *pnp* transistor. Both are shown in figure 3.1 with proper biasing.

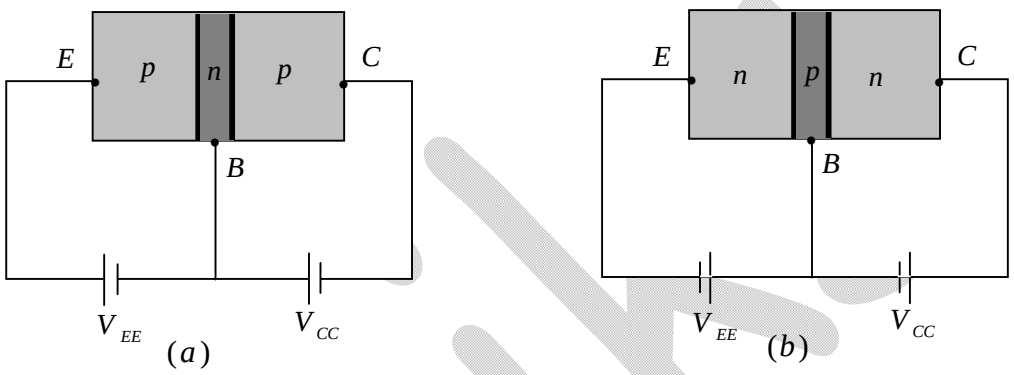


Figure 3.1: Types of transistors: (a) *pnp* (b) *npn*.

The emitter layer is heavily doped, the base lightly doped, and the collector only lightly doped. The outer layers have widths much greater than the sandwiched *p*- or *n*-type material. The ratio of the total width to that of the center layer is 150:1. The doping of the sandwiched layer is also considerably less than that of the outer layer (typically, 10:1 or less).This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of "free" carriers.

The terminals have been indicated by the capital letters *E* for *emitter*, *C* for *collector*, and *B* for *base*. The term bipolar junction transistor (BJT) reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material.

3.2 Transistor Operation

The basic operation of the transistor is described using *pnp* transistor as shown in figure 3.1(a). The operation of the *npn* transistor is exactly the same if the roles played by the electron and holes are interchanged. In figure 3.2 the *pnp* transistor has been redrawn without the base-to-collector bias (similar to *forward-biased* diode). The depletion region has been reduced in width due to applied bias, resulting in a heavy flow of majority carriers from *p*- to the *n*-type material.

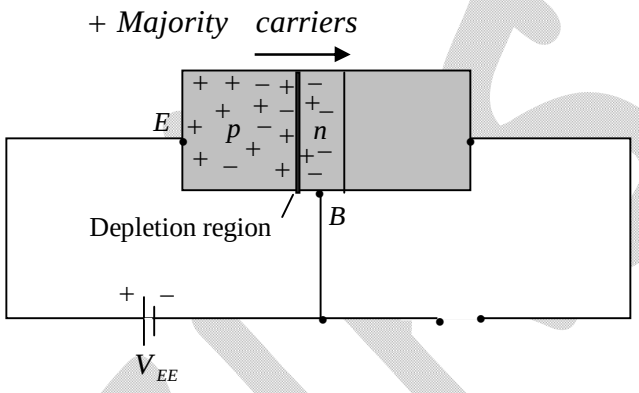


Figure 3.2: Forward-biased junction of a *pnp* transistor.

Let us now remove the base-to-emitter bias of the *pnp* transistor of figure 3.1(a) as shown in figure 3.3 (similar to *reverse-biased* diode). Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow. Thus

"One p-n junction of a transistor is reversed biased, while the other is forward biased."

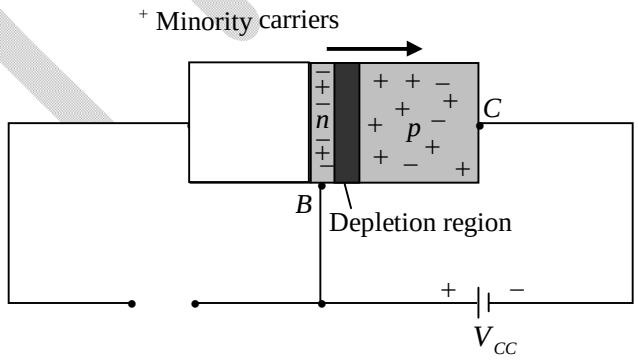


Figure 3.3: Reverse based junction of a *pnp* transistor.

In figure 3.4 both biasing potentials have been applied to a *pnp* transistor, with the resulting majority and minority-carrier flow indicated. The widths of the depletion regions, indicating clearly which junction is forward-biased and which is reversed-biased. A large number of majority carriers will diffuse across the forward-biased *p*-*n* junction into the *n*-type material. Since *n*-type material is very thin and has low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal. The larger number of these majority carriers will diffuse across the reverse-biased junction into the *p*-type material connected to the collector terminal. Thus there has been an *injection* of minority carriers into the *n*-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reversed-biased junction of a diode accounts for the flow indicated in the figure 3.4.

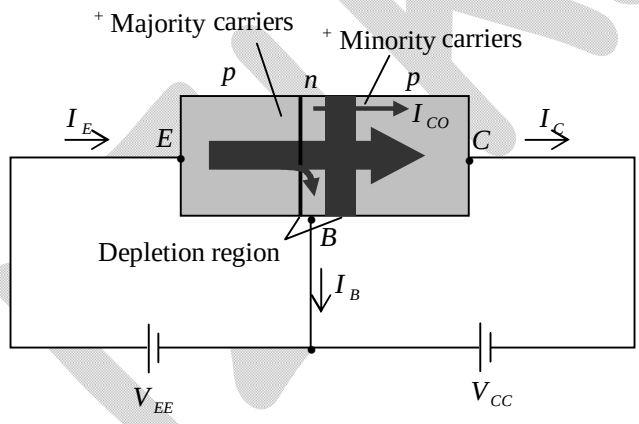


Figure 3.4: Majority and minority carrier flow of a *pnp* transistor.

Applying Kirchhoff's current law to the transistor of figure 3.4 as if it were a single node, we obtain

$$I_E = I_C + I_B$$

The minority current component is called the leakage current and is given by the symbol I_{CO} (collector current with emitter terminal open). The collector current, therefore is:

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$$

3.3 Transistor Configurations

3.3.1 Common-Base Configuration

The common-base configuration with *pnp* and *npn* transistors are shown in figure 3.5. The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configurations.

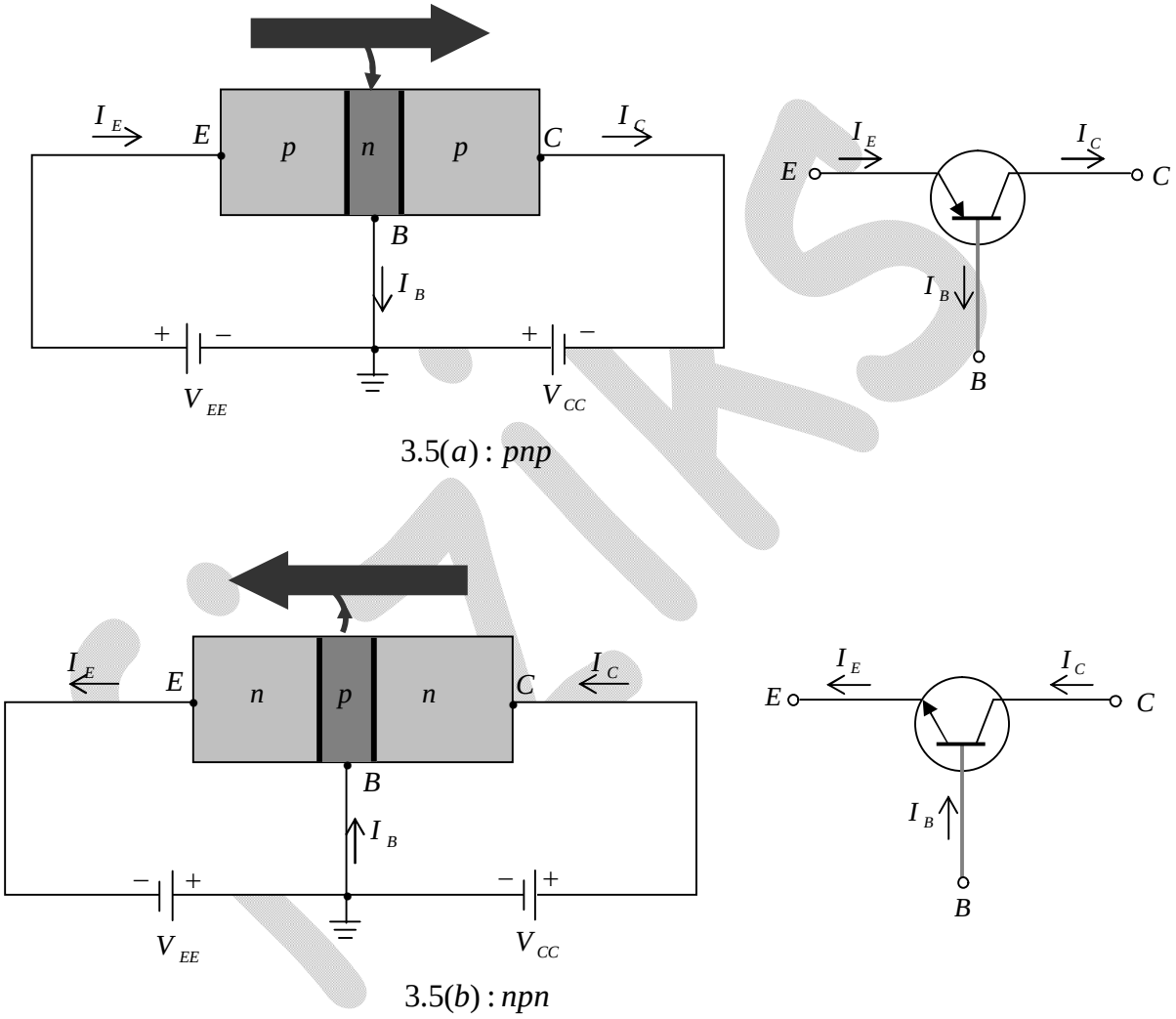


Figure 3.5: Notation and symbols used with the common base-configuration:
(a) *pnp* transistor; (b) *npn* transistor.

To fully describe the behavior of a three terminal device such as common base amplifiers requires two set of characteristics- one for the *driving point* or *input* parameters and the other for the *output* side.

Input Characteristics

The input set for the common base amplifiers as shown in figure 3.6 will relate an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

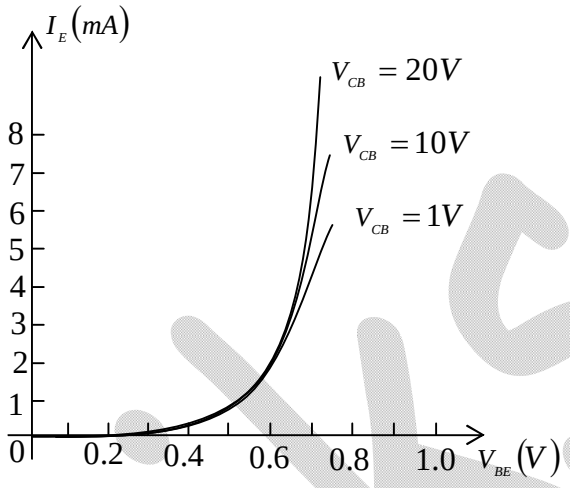


Figure 3.6: Input or driving point characteristics for a common-base silicon transistor.

Output Characteristics

The output set will relate an output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E). The output characteristics have three basic regions of interest: the ***active***, ***cutoff***, and ***saturation*** regions. The active region is the region normally employed for linear (undistorted) amplifiers.

In the active region the collector-base junction is reversed-biased, while the base-emitter junction is forward biased.

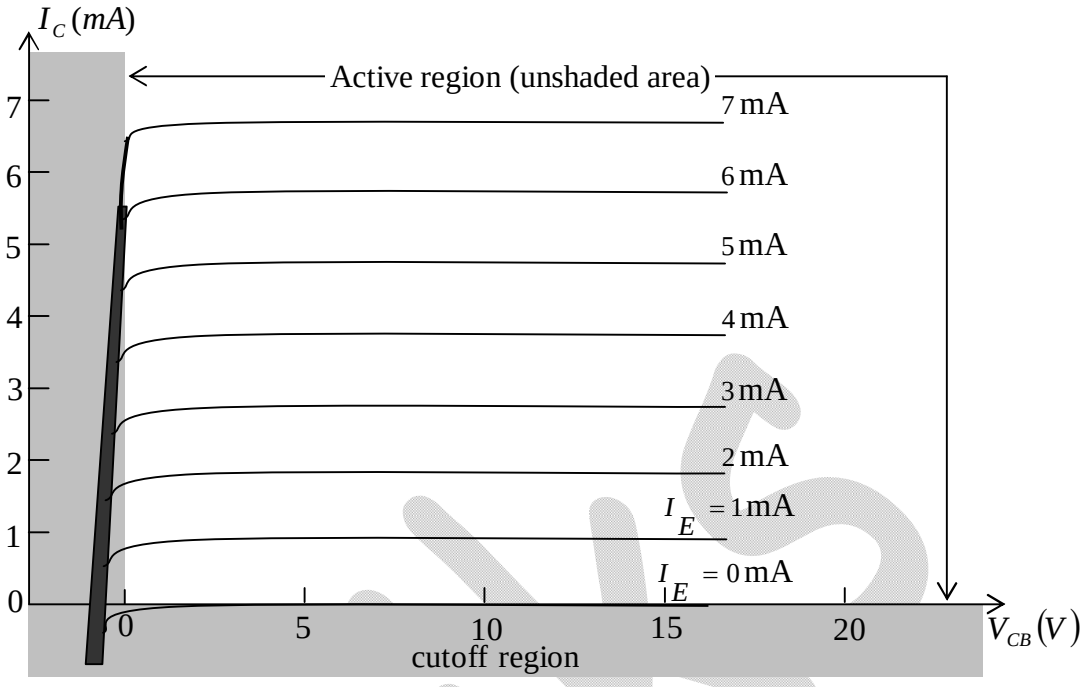


Figure 3.7: Output or collector characteristics for a common-base transistor amplifier.

The circuit condition that exists when $I_E = 0$ for common base configuration is shown in figure 3.8. Note that I_{CBO} is temperature dependent and increases so rapidly with temperature.

In the output characteristics as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor current relations. Note also the almost negligible effect of V_{CB} on the collector current for the active region.

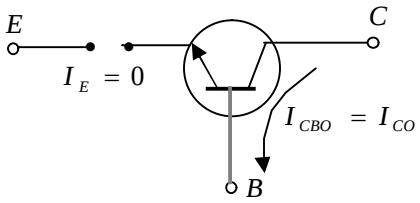


Figure 3.8: Reverse Saturation current.

In the cutoff region the collector-base and base-emitter junctions are both reversed-biased.

In the saturation region the collector-base and base-emitter junctions are both forward-biased.

Alpha (α)

In the dc mode the levels of I_C and I_E due to majority carriers are related by a quantity called *alpha* and defined by the following equations:

$\alpha_{dc} = \dfrac{I_C}{I_E}$ where I_C and I_E are the levels of current at the point of operation.

Thus $I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}} \Rightarrow I_C = \alpha I_E + I_{CBO}$

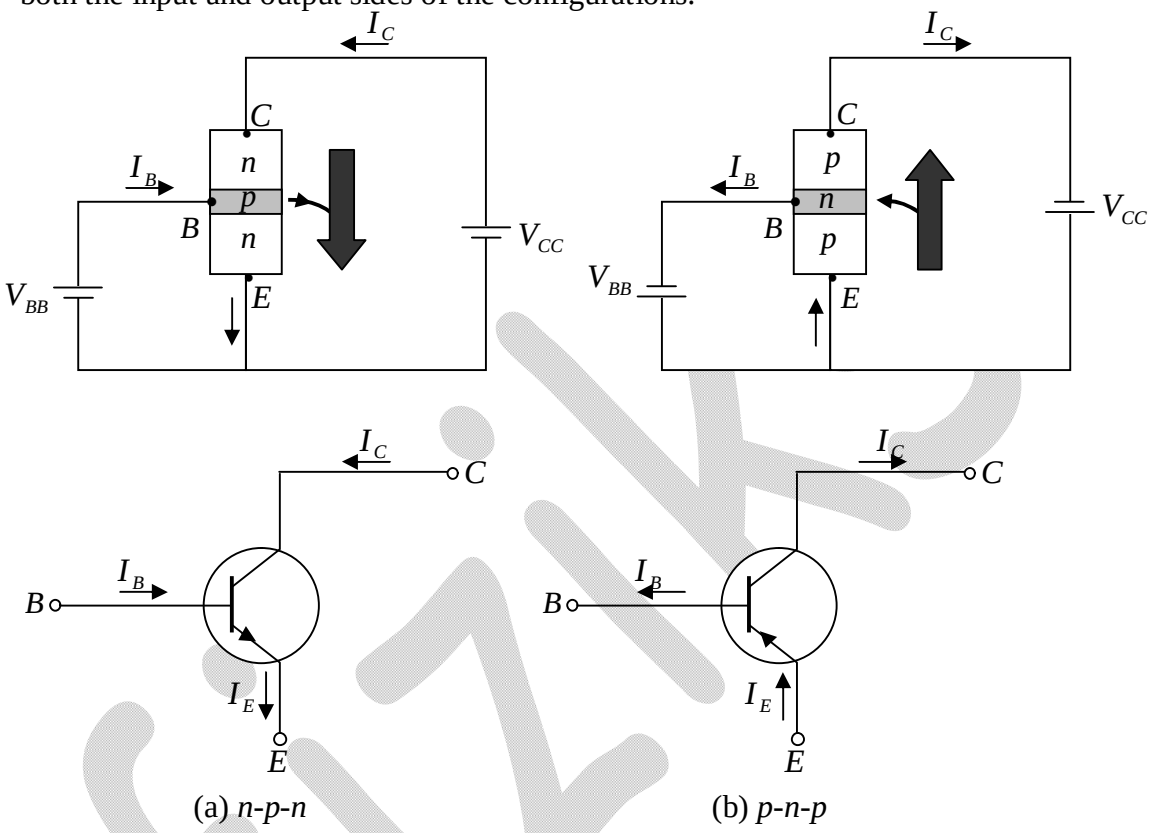
For ac situations where the point of operation moves on the characteristics curve, an ac *alpha* is defined by $\alpha_{ac} = \left.\dfrac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$.

The ac alpha is formally called the *common-base, short-circuit, amplification factor*.

The typical values of *voltage amplification* $\left(V_o/V_i\right)$ for the common-base configuration vary from 50 to 300. The *current amplification* $\left(I_C/I_E\right)$ is always less than 1 for the common-base configuration.

3.3.2 Common Emitter Configuration

The common-emitter configuration with *pnp* and *npn* transistors are shown in figure 3.9. The common-emitter terminology is derived from the fact that the emitter is common to both the input and output sides of the configurations.



(a) *n-p-n* (b) *p-n-p*

Figure 3.9: Notation and symbols used with the common-emitter configuration.

To fully describe the behavior of a three terminal device such as common emitter amplifier requires two set of characteristics- one for the *input* or *base-emitter* circuit and one for the *output* or *collector-emitter* circuit.

The output characteristics will relate an output current (I_C) to an output voltage (V_{CE}) for various levels of input current (I_B). The input characteristics for the common emitter amplifiers will relate an input current (I_B) to an input voltage (V_{BE}) for various levels of output voltage (V_{CE}).

In the active region the collector-base junction is reversed-biased, while the base-emitter junction is forward biased.

In the cutoff region the collector-base and base-emitter junctions are both reversed-biased.

In the saturation region the collector-base and base-emitter junctions are both forward-biased.

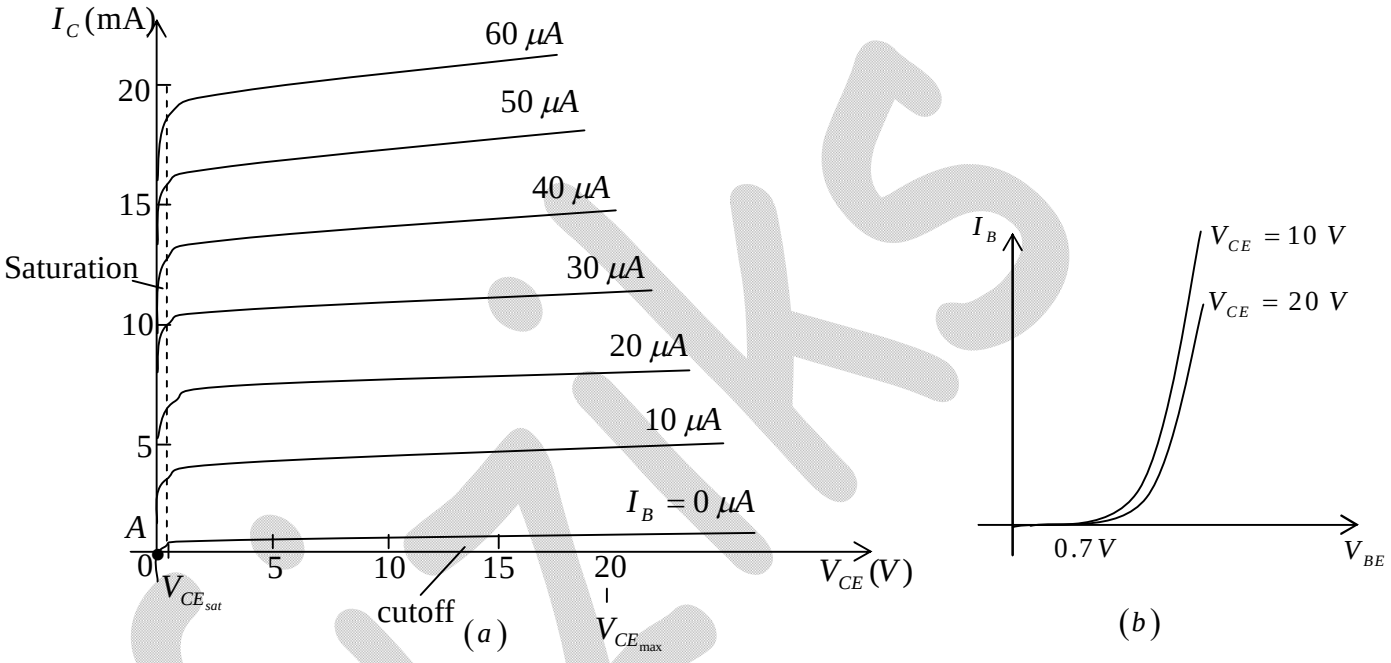


Figure 3.10: Characteristics of a silicon transistor in the common emitter configuration: (a) Collector characteristics; (b) base characteristics.

Since $I_C = \alpha I_E + I_{CBO} = \alpha(I_C + I_B) + I_{CBO} \Rightarrow I_C = \dfrac{\alpha I_B}{1-\alpha} + \dfrac{I_{CBO}}{1-\alpha}$

or $I_C = \beta I_B + I_{CEO}$ where $I_{CEO} = \left.\dfrac{I_{CBO}}{1-\alpha}\right|_{I_B=0}$ and $\beta = \dfrac{\alpha}{1-\alpha}$.

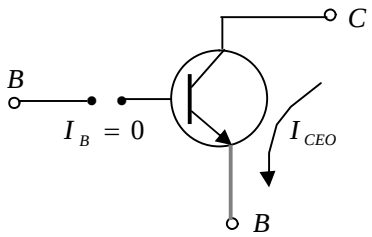


Figure 3.11: Circuit condition related to I_{CEO}.

Beta (β)

In the dc mode the levels of I_C and I_B are related by a quantity called *beta* and defined by the following equations: $\beta_{dc} = \frac{I_C}{I_B}$ where I_C and I_B are the levels of current at the point of operation. For ac situations where the point of operation moves on the characteristics curve, an ac beta is defined by $\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}$. The formal name for β_{ac} is *common emitter forward-current amplification factor*.

3.3.3 Common-Collector Configuration

The third and final transistor configuration is the common–collector configuration, shown in figure 3.12 with the proper current directions and voltage notation. The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

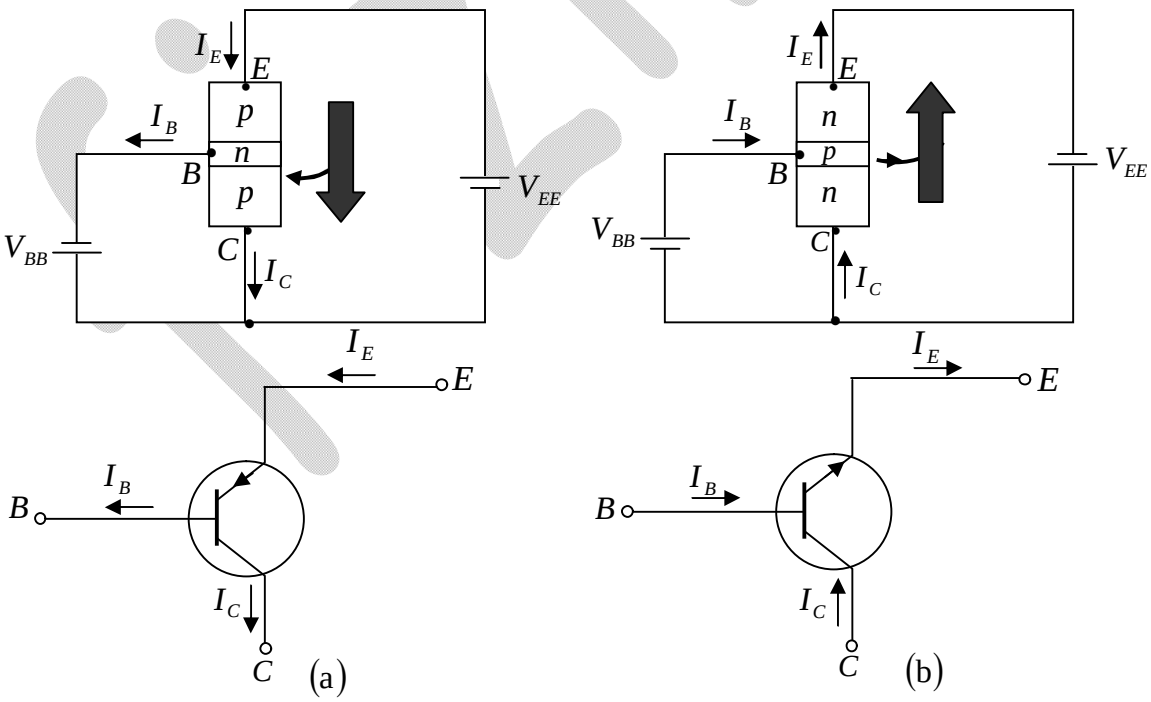


Figure 3.12: Notation and symbols used with the common-collector configuration.

A common collector circuit configuration is provided in figure 3.13 with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common emitter configuration. For all practical purposes, the output characteristics of the CC configuration are same as for the CE configuration.

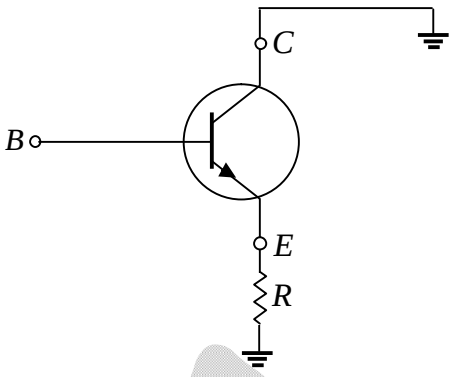


Figure 3.13: Common-collector configuration.

3.4 DC Biasing-BJTs

3.4.1 Introduction

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. The improved output ac power level is the result of a transfer of energy from the applied dc supplies. The analysis or design of any electronic amplifier, therefore, has two components: the *dc portion* and the *ac portion*. Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design stage the choice of parameters for the required dc levels will affect the ac response and vice-versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations.

Although a number of networks will be analyzed, there is an underlying similarly between the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$V_{BE} = 0.7V,\ I_E = (\beta + 1) I_B \cong I_C \text{ and } I_C = \beta I_B$$

3.4.2 Operating Point

Since the operating point is a fixed point on the characteristics it is also called the quiescent point (abbreviated *Q-point*). By definition, quiescent means quiet, still, inactive. Figure 3.14 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the active region. The maximum ratings are indicated on the characteristics by a horizontal line for the maximum collector current $I_{C_{max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE_{max}}$. The maximum power constraint is defined by the curve $P_{C_{max}}$ in the same figure. At the lower end of the scales are the *cutoff regions*, defined by $I_B \le 0\ \mu A$ and the *saturation region*, defined by $V_{CE} \le V_{CE_{sat}}$.

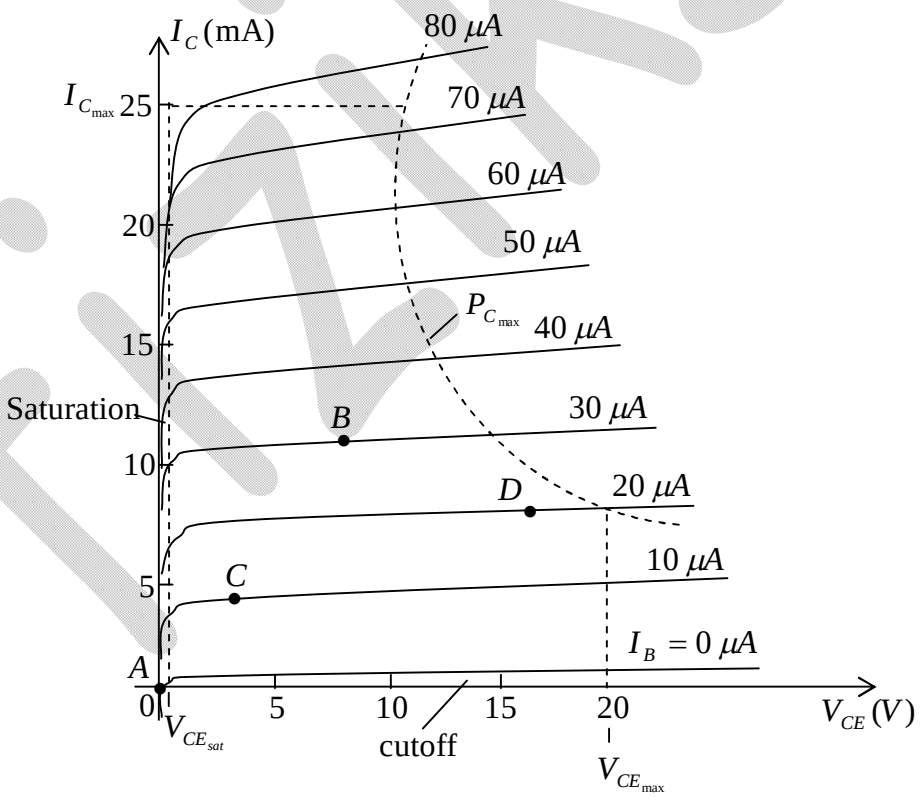


Figure 3.14: Various operating points within the limits of operation of a transistor.

If no bias were used, the device would initially be completely off, resulting in a *Q*-point at **A**-namely zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal *point A* would not be suitable. For ***point B*** if a signal is applied to the circuit, the device will vary in current and voltage from operating point, allowing the device to react to both the positive and negative excursion of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary but not enough to drive the device into cutoff or saturation. ***Point C*** would allow some positive and negative variation of the output signal but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0\ V$, $I_C = 0\ mA$. Operating at point C also raise some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region.

In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. ***Point D*** sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. ***Point B*** is a region of more linear spacing and therefore, seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers but not the case necessarily for power amplifiers. In this discussion, we will be concentrating primarily on biasing the transistor for *small-signal amplification operation*.

Having selected and biased the BJT at a desired operating point, the *effect of temperature* must also be taken into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of temperature stability so that temperature changes result in minimum changes in the operating point.

This maintenance of the operating point can be specified by a stability factor, *S*, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:

1. The base-emitter junction must be forward-biased (*p*-region voltage more positive) with a resulting forward-bias voltage of about 0.6 to 0.7 *V*.
2. The base-collector junction must be reverse-biased (*n*-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

Operation in the cutoff, saturation and linear regions of the BJT characteristic are provided as follows:

1. Linear-region operation:

   Base-emitter junction forward biased

   Base-collector junction reversed biased

2. Cutoff-region operation:

   Base-emitter junction reverse biased

   Base-collector junction reversed biased

3. Saturation-region operation:

   Base-emitter junction forward biased

   Base-collector junction forward biased

3.5 Fixed-Bias Circuit

The fixed-bias circuit of figure 3.15 provides a relatively straightforward and simple introduction to transistor dc bias analysis. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and the voltage polarities.

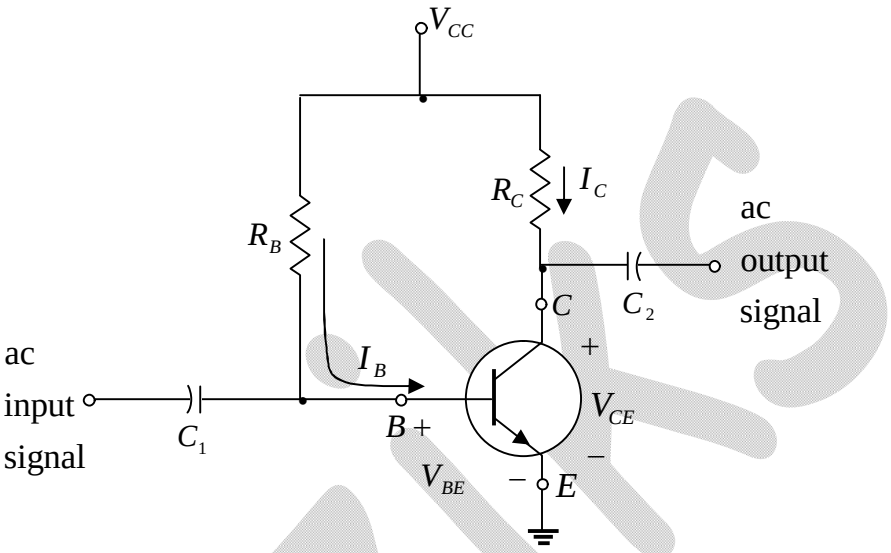


Figure 3.15: Fixed-bias circuit

For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in figure 3.16 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B.

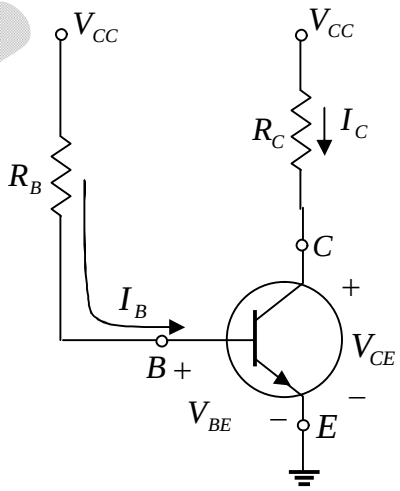


Figure 3.16: DC equivalent of figure 3.15.

3.5.1 Q-Point

Forward Bias of Base-Emitter

Consider first the base-emitter circuit loop of figure shown 3.17. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain $-V_{CC} + I_B R_B + V_{BE} = 0$

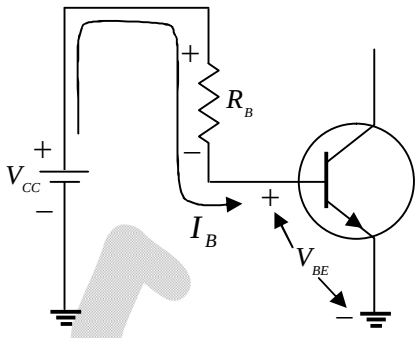


Figure 3.17: Base-emitter loop.

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B will result in the following: $I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$

Since the supply voltage V_{CC} and the base-emitter voltage V_{BE} are constants, the selection of a base resistor, R_B sets the level of base current for the operating point.

Collector-Emitter Loop

The collector-emitter section of the network appears in figure 3.18 with the indicated direction of current I_C and the resulting polarity across R_C.

The magnitude of the collector current is related directly to I_B through

$$I_C = \beta I_B$$

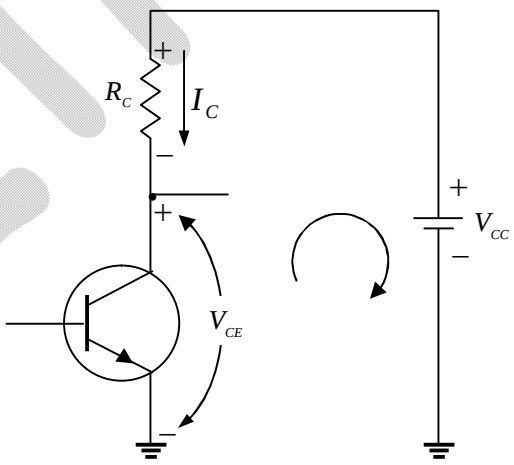


Figure 3.18: Collector-emitter loop.

It is interesting to note that since the base current is controlled by the level of R_B and I_C is related to I_B by a constant β the magnitude of I_C is not a function of the resistance R_C. Change R_C to any level and it will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed-loop of figure 3.18 will result in the following:

$$-V_{CC} + I_C R_C + V_{CE} = 0 \Rightarrow V_{CE} = V_{CC} - I_C R_C$$

As a brief review of single and double subscript notation recall that

$$V_{CE} = V_C - V_E$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground respectively. But in this case since $V_E = 0\ V$, we have

$$V_{CE} = V_C .$$

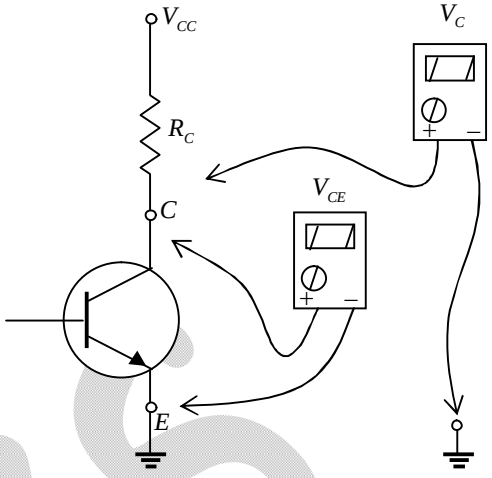


Figure 3.19: Measuring V_{CE} and V_C.

In addition, since $V_{BE} = V_B - V_E$ and $V_E = 0\ V$ then $V_{BE} = V_B$.

Keep in mind that voltage levels such as V_{CE} are determined by placing the positive lead of the voltmeter at the collector terminal with the negative lead at the emitter terminal as shown in figure 3.19. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different.

3.5.2 Transistor Saturation

The term saturation is applied to any system where levels have reached their maximum values. For a transistor operating in the saturation region the current is a maximum value for the particular design. Change the design and the corresponding saturation level may rise or drop.

Saturation conditions are normally avoided because the base-collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation region is depicted in figure 3.20. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE_{sat}}$. In addition, the collector current is relatively high on the characteristics.

If we approximate the curves of figure 3.20(a) by those appearing in figure 3.20(b), a quick direct method for determining the saturation level becomes apparent. In figure 3.20(b) the current is relatively high and the voltage V_{CE} is assumed to be zero volts. Applying Ohm's law the resistance between collector and emitter terminals can be determined as follows: $R_{CE} = \frac{V_{CE}}{I_C} = \frac{0V}{I_{C_{sat}}} = 0\Omega$

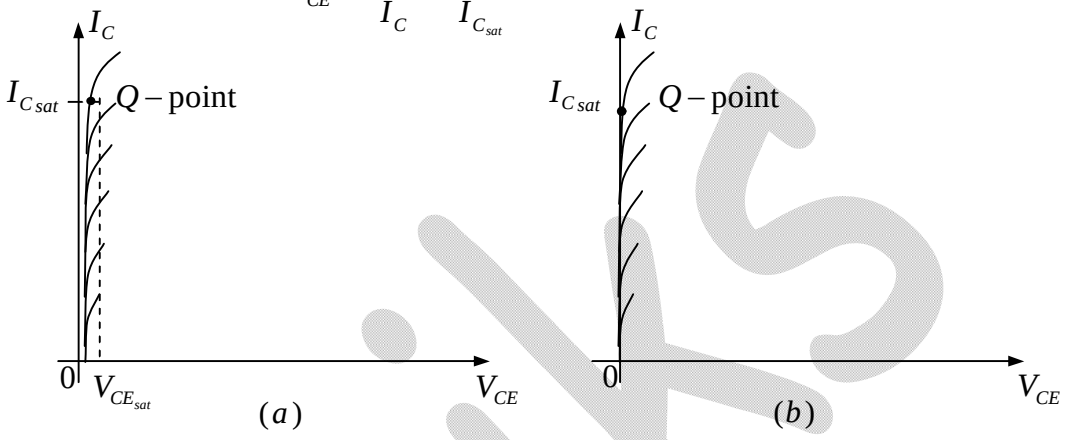


Figure 3.20: Saturation region (a) actual (b) approximate.

For saturation current set $V_{CE} = 0\,V$ and find $I_{C_{sat}}$. For the fixed-bias configuration of figure 3.22 the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}. The resulting saturation current for the fixed-bias configuration is

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

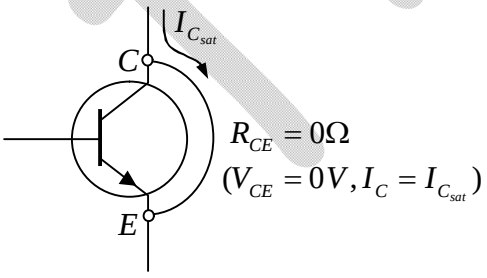


Figure 3.21: Determining $I_{C_{sat}}$

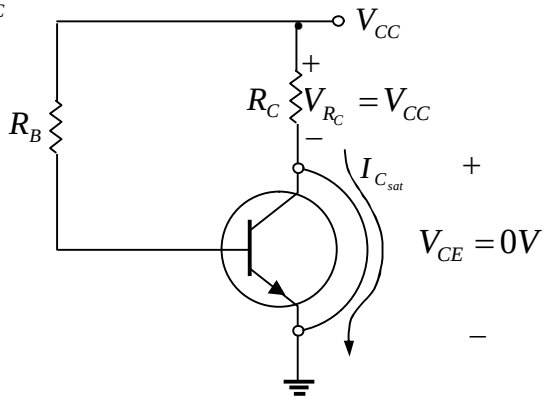


Figure 3.22: $I_{C_{sat}}$ for the fixed-bias configuration.

3.5.3 Load-Line Analysis

We will now investigate how the network parameters define the possible range of *Q*-points and how the actual *Q*-point is determined.

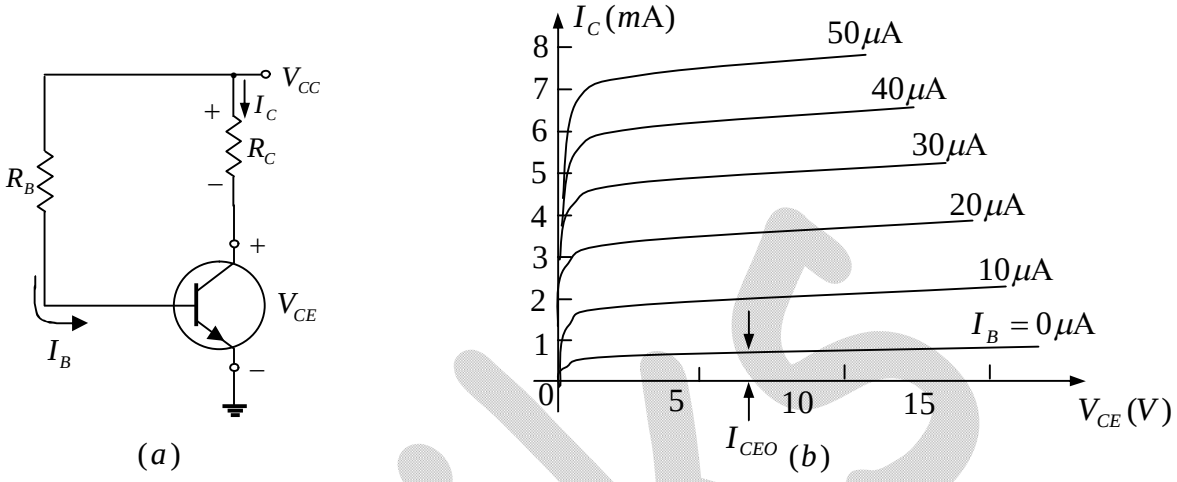


Figure 3.23: Load-line analysis (a) the network (b) the device characteristics.

The network of figure 3.23(a) establishes an output equation that relates the variables I_C and V_{CE} in the following manner: $V_{CE} = V_{CC} - I_C R_C$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} in figure 3.23(b).

We must now superimpose the straight line defined by equation $V_{CE} = V_{CC} - I_C R_C$ on the characteristics. If we choose I_C to be $0\ mA$, we are specifying the horizontal axis as the line on which one point is located. By substituting $I_C = 0\ mA$, we find that $V_{CE} = V_{CC}\big|_{I_C = 0\ mA}$ defining one point for the straight line as shown in figure 3.24.

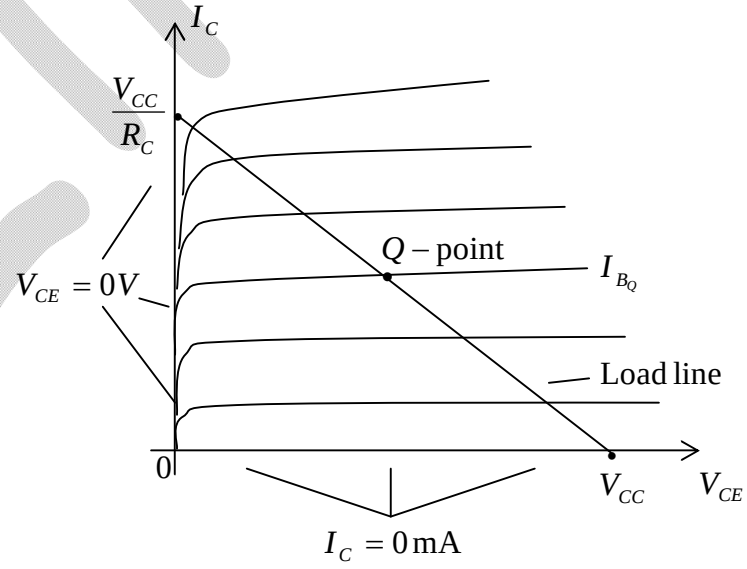


Figure 3.24: Fixed-bias load.

If we now choose V_{CE} to be $0\,V$, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$0 = V_{CC} - I_C R_C \quad \text{and} \quad I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0V} \text{ as appearing on figure 3.24.}$$

By joining the two points defined by equation $V_{CE} = V_{CC}\big|_{I_C=0mA}$ and $I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0V}$ the straight line established by equation $V_{CE} = V_{CC} - I_C R_C$ can be drawn. The resulting line on the graph of figure 3.24 is called the ***load line*** since it is defined by the load resistor R_C. By solving for the resulting level of I_B the actual *Q*-point can be established.

If the level of I_B is changed by varying the value of R_B the *Q*-point moves up or down the load line as shown in figure 3.25.

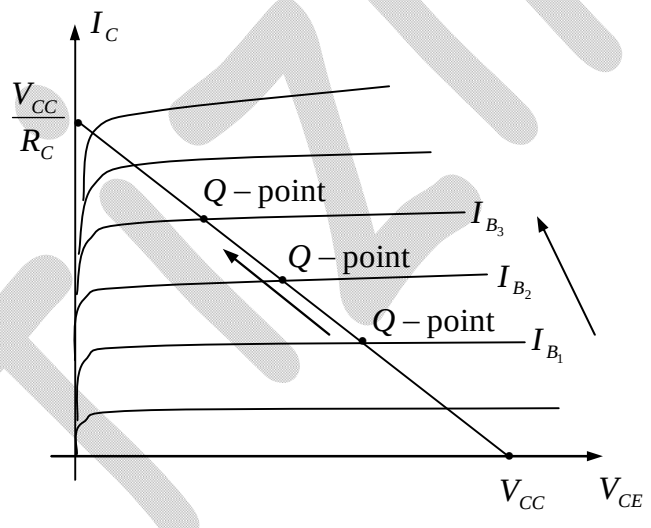


Figure 3.25: Movement of *Q*-point with increasing levels of I_B.

NOTE: For Fixed R_B if temperature of the device increases the *Q*-point will moves towards the saturation region as shown in figure 3.25. Since $I_C = \beta I_B + I_{CEO}$ with increase in temperature reverse current $I_{CEO} = (\beta +) I_{CBO}$ increases.

If V_{CC} is held fixed and R_C changed, the load line will shift as shown in figure 3.26. If I_B is held fixed, the Q-point will move as shown in the same figure.

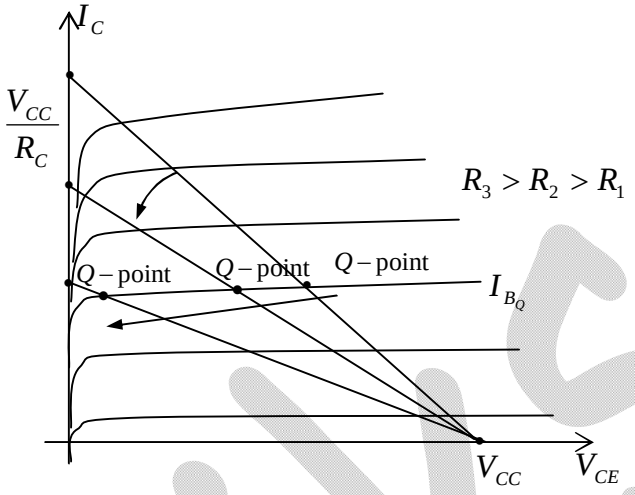


Figure 3.26: Effect of increasing levels of R_C on the load line and Q-point.

If R_C is fixed and V_{CC} varied, the load line shifts as shown in figure 3.27.

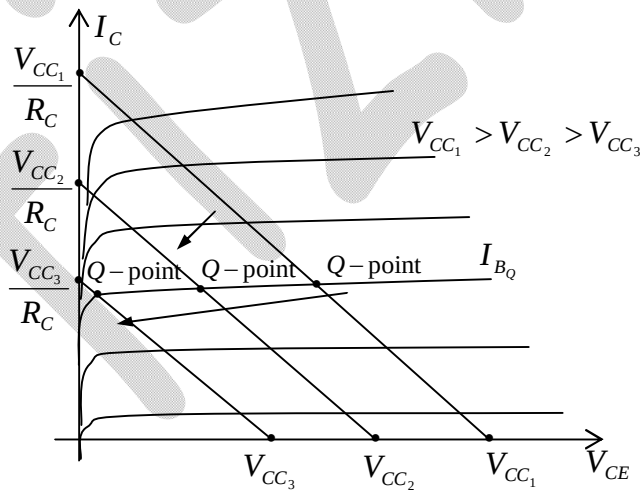
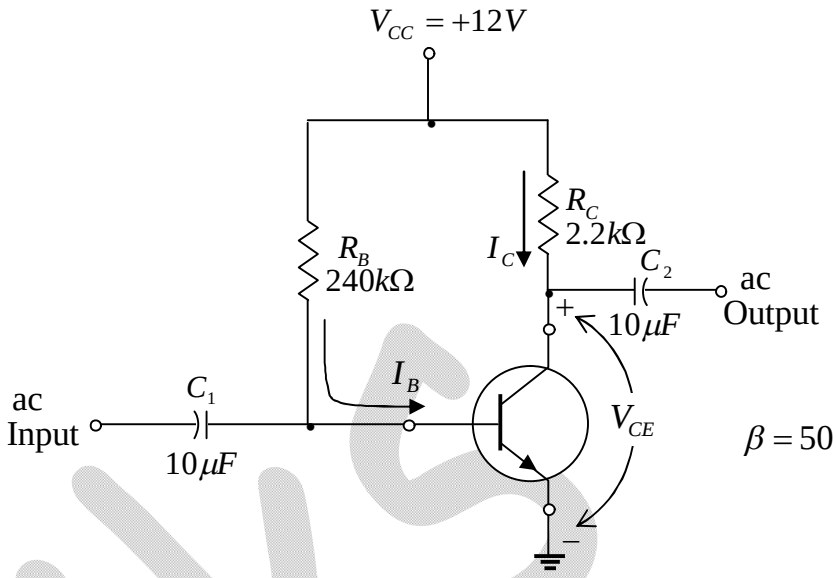


Figure 3.27: Effect of lower values of V_{CC} on the load line and Q-point.

Example: Determine the following for the fixed-bias configuration of figure shown below.



(a) I_{B_Q} and I_{C_Q}

(b) V_{CE_Q}

(c) V_B and V_C

(d) V_{BC}

(e) Saturation level.

Solution:

(a) $I_{B_Q} = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12V - 0.7V}{240\,k\Omega} = 47.08\,\mu A$

$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\,\mu\text{A}) = 2.35\,m\text{A}$

(b) $V_{CE_Q} = V_{CC} - I_C R_C = (12)(2.35\,mA)(2.2\,k\Omega) = 6.83\,V$

(c) $V_B = V_{BE} = 0.7\ V$

$V_C = V_{CE} = 6.83\ V$

(d) Using double-subscript notation yields

$V_{BC} = V_B - V_C = 0.7\ V - 6.83\ V = -6.13\ V$

With the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

(e) $I_{c_{sat}} = \dfrac{V_{CC}}{R_C} = \dfrac{12V}{2.2\,k\Omega} = 5.45\,m\text{A}$

$I_{C_Q} = 2.35\,m\text{A}$, which is far from the saturation level and about one-half the maximum value for the design.

3.6 Emitter-Stabilized Bias Circuit

The dc bias network of figure 3.28 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.

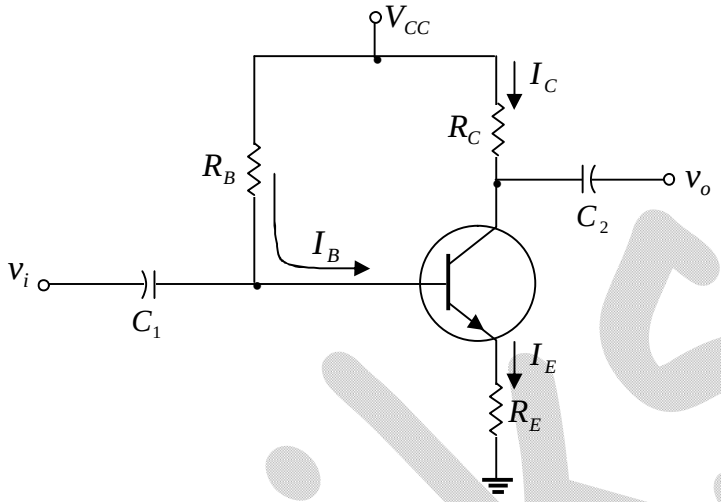


Figure 3.28: BJT circuit with emitter resistor.

3.6.1 *Q*-Point

The analysis will be performed by first examining the base-emitter loop and then using the results to investigate the collector-emitter loop.

Base–Emitter Loop

The base-emitter loop of the network can be redrawn as shown in 3.29. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in the following equation:

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0 \quad \because I_E = (\beta + 1) I_B$$

Grouping terms will then provide the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}.$$

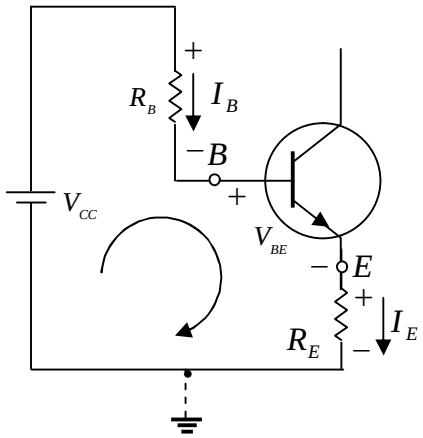


Figure 3.29: Base-emitter loop.

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(\beta + 1) R_E$.

There is an interesting result that can be derived from equation $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ if the equation is used to sketch a series network that would result in the same equation. Such is the case for the network of figure 3.30. Solving for the current I_B will result in the same equation obtained above. Note that aside from the base-to-emitter voltage V_{BE} the resistor R_E is reflected back to the input base circuit by a factor $(\beta + 1)$. In other words, the emitter resistor, which is part of the collector–emitter loop, "appears as" $(\beta + 1)R_E$ in the base-emitter loop. Since β is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit.

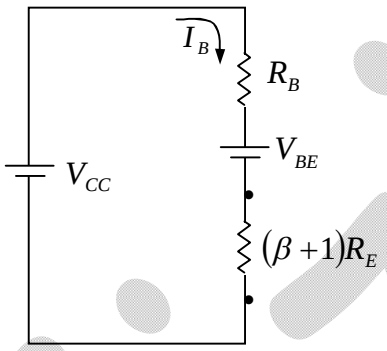


Figure 3.30: Network derived from I_B.

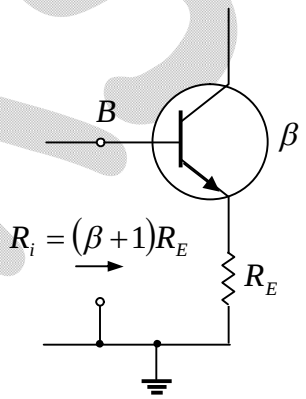


Figure 3.31: Reflected impedance level of R_E.

In general, therefore, for the configuration of figure 3.31,

$$R_i = (\beta + 1)R_E$$

This equation is one that will prove useful in the analysis to follow. In fact, it provides a fairly easy way to remember equation $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$. Using Ohm's law, we know that the current through a system is the voltage divided by the resistance of the circuit. For the base-emitter circuit the net voltage is $V_{CC} - V_{BE}$. The resistance levels are R_B plus R_E reflected by $(\beta + 1)$.

Collector–Emitter Loop

The collector-emitter loop is redrawn in figure 3.32.

Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction will result in

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_C \approx I_E$ and grouping terms gives

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E$$

while the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E \quad \text{or} \quad V_C = V_{CE} + V_E \quad \text{and} \quad V_C = V_{CC} - I_C R_C$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_B \quad \text{or} \quad V_B = V_{BE} + V_E$$

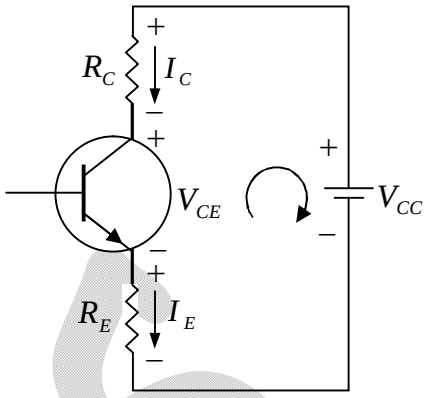


Figure 3.32: Collector-emitter loop.

3.6.2 Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

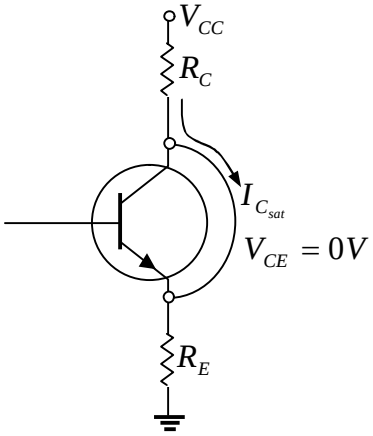


Figure 3.33: Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.

3.6.3 Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I_B as determined by equation $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ defines the level of I_B on the characteristics of figure 3.34 (denoted I_{B_Q}).

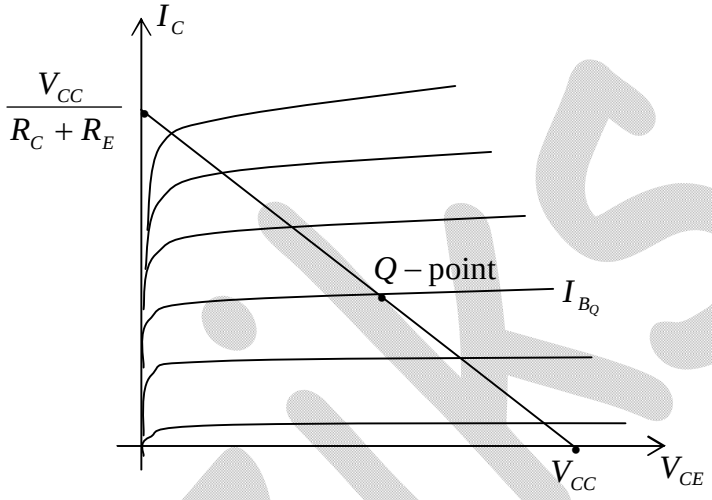


Figure 3.34: Load-Line for the emitter-bias configuration.

The collector-emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$V_{CE} = V_{CC}\big|_{I_C = 0\,V}$$

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0\ V$ gives

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0V}$$

as shown in figure 3.34. Different levels of I_{B_Q} will, of course, move the *Q*-point up or down the load line.

Example: For the emitter bias network of figure shown below, determine:

(a) I_B

(b) I_C

(c) V_{CE}

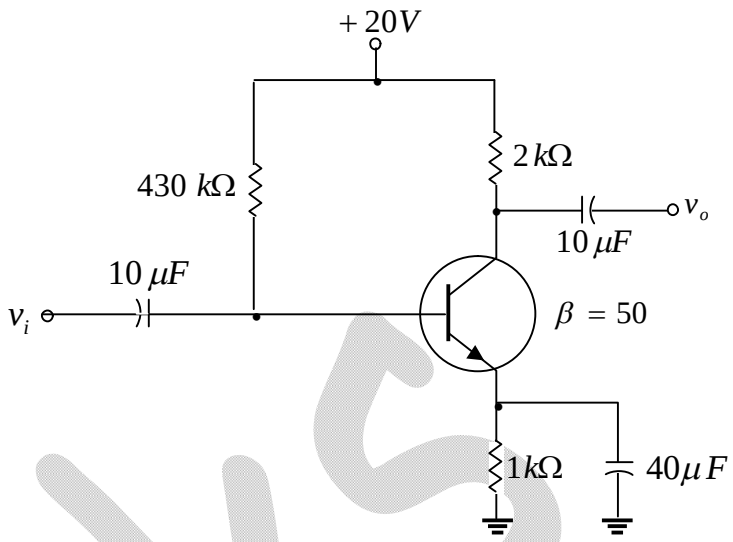
(d) V_C

(e) V_E

(f) V_B

(g) V_{BC}

(h) $I_{C_{sat}}$



Solution:

(a) $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \dfrac{20V - 0.7V}{430\,k\Omega + (51)(1k\Omega)} = \dfrac{19.3\ V}{481\ \ k\Omega} = 40.1\ \ \mu A$

(b) $I_C = \beta I_B = (50)(40.1\ \ \mu A) = 2.01\ mA$

(c) $V_{CE} = V_{CC} - I_C(R_C + R_E) = (20) - (2.01mA)(2k\Omega + 1k\Omega) = 13.97\ V$

(d) $V_C = V_{CC} - I_C R_C = (20) - (2.01mA)(2k\Omega) = 15.98\ V$

(e) $V_E = V_C - V_{CE} = 15.98\ V - 13.97V = 2.01\ V$

(f) $V_B = V_{BE} + V_E = 0.7\ V + 2.01V = 2.71\ V$

(g) $V_{BC} = V_B - V_C = 2.71\ V - 15.98V = -13.27\ V$ (reverse-biased as required)

(h) $I_{C_{sat}} = \dfrac{V_{CC}}{R_C + R_E} = \dfrac{20\ \ V}{2k\Omega\ \ +\ \ 1\ \ k\Omega} = \dfrac{20\ \ V}{3\ \ k\Omega} = 6.67\ mA$

which is about twice the level of I_{C_Q}.

3.7 Voltage-Divider Bias

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain (β) of the transistor. However, since β is temperature sensitive, specially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in fact, independent of the transistor beta.

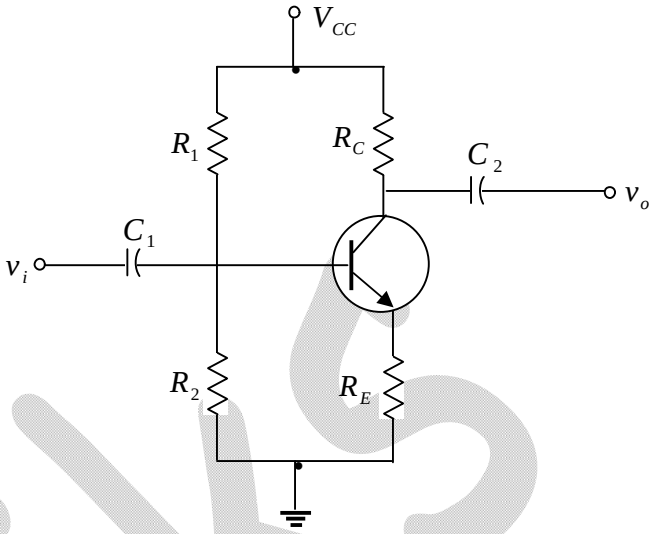


Figure 3.35: Voltage-divider bias configuration.

The voltage-divider bias configuration of figure 3.35 is such a network. If analyzed on an exact basis the sensitivity to changes in beta is quite small.

3.7.1 *Q*-point

The input side of the network can be redrawn as shown in figure 3.36 for the dc analysis. The Thevenin equivalent network for the network to the left of the base terminal can then be found in the following manner.

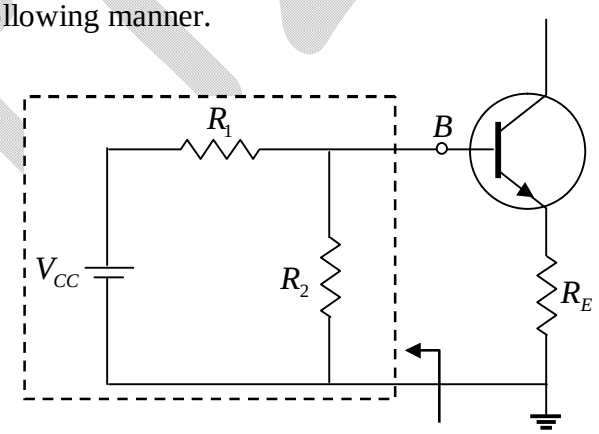


Figure 3.36: Redrawing the input side of the network of figure 3.35.

Thevenin's Resistance (R_{Th}):

The voltage source is replaced by a short-circuit equivalent as shown in figure 3.37.

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

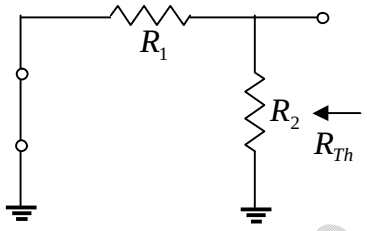


Figure 3.37: Determining R_{TH}.

Thevenin's Voltage (E_{Th}):

The voltage source V_{CC} is returned to the network and the open-circuit Thevenin voltage of figure 3.38 determined as follows:

Applying the voltage-divider rule:

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

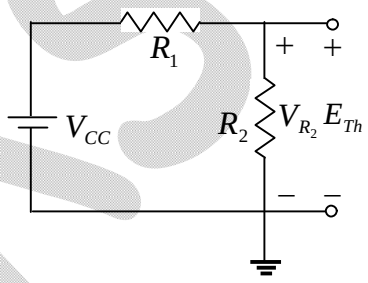


Figure 3.38: Determining E_{TH}.

The Thevenin network is then redrawn as shown in figure 3.39 and I_{B_Q} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated: $-E_{Th} + I_B R_{Th} + V_{BE} + I_E R_E = 0$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \qquad \because I_E = (\beta +) I_B$$

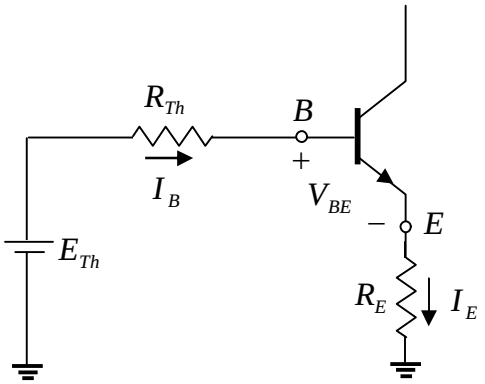


Figure 3.39: Thevenin equivalent circuit.

Once I_B is known the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is $V_{CE} = V_{CC} - I_C(R_C + R_E)$.

The remaining equations for V_E, V_C and V_B are also the same as obtained for the emitter-bias configuration.

3.8.2 Transistor Saturation

The output collector-emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit. The resulting equation for the saturation current (when V_{CE} is set to zero volts on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is, $I_{C_{sat}} = I_{C_{max}} = \dfrac{V_{CC}}{R_C + R_E}$.

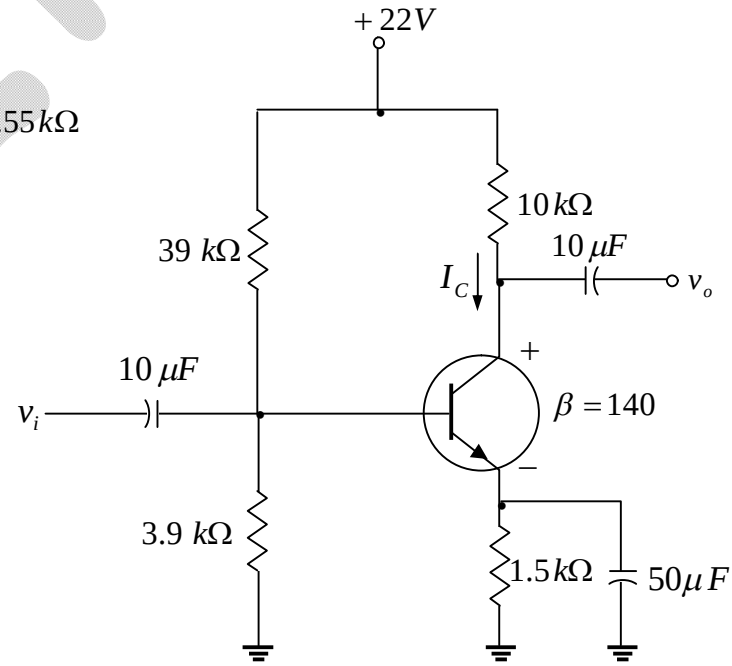
3.8.3 Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of figure 3.24, with

$$I_{C_{sat}} = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0V} \quad \text{and} \quad V_{CE} = V_{CC}\big|_{I_C=0mA}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

Example: Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of figure shown below.



Solution: $R_{TH} = R_1 \,||\, R_2 = \dfrac{(39k\Omega)(3.9k\Omega)}{39k\Omega + 3.9k\Omega} = 3.55k\Omega$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\,k\Omega)(22V)}{39\,k\Omega + 3.9\,k\Omega} = 2V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{2V - 0.7V}{3.55\,k\Omega + (141)(1.5\,k\Omega)}$$

$$\Rightarrow I_B = \frac{1.3V}{3.55\ \ k\Omega + 211.5\ \ k\Omega} = 6.05\ \mu A$$

$$\Rightarrow I_C = \beta I_B = (140)(6.05\ \mu A) = 0.85\ mA$$

$$\because V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$\Rightarrow V_{CE} = 22 - (0.85\,mA)(10k\Omega + 1.5k\Omega) = 12.22\ V$$

3.8 DC Bias with Voltage Feedback

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in figure 3.40.

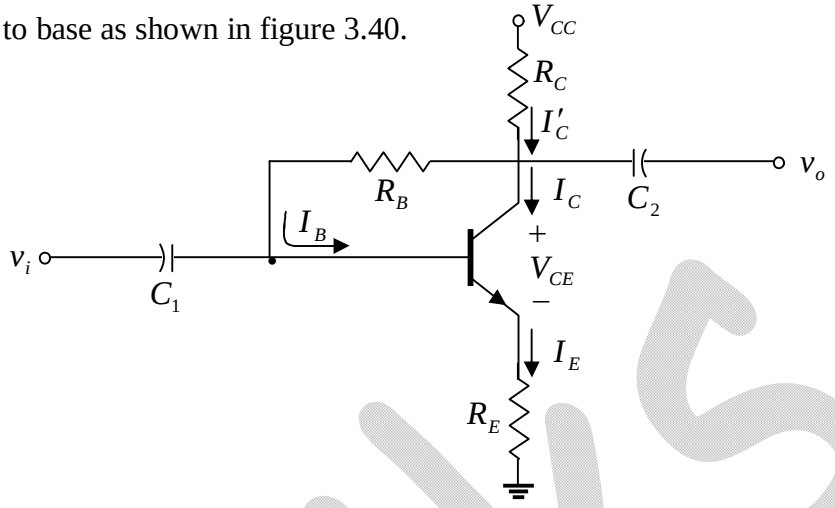


Figure 3.40: DC Bias with voltage feedback.

3.8.1 *Q*-point (Base-Emitter Loop)

Figure 3.41 shows the base-emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$-V_{CC} + I'_C R_C + I_B R_B + V_{BE} + I_E R_E = 0$$

It is important to note that the current through R_C is not I_C but I'_C (where $I'_C = I_C + I_B \approx I_C$). Thus

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta\left(R_C + R_E\right)}.$$

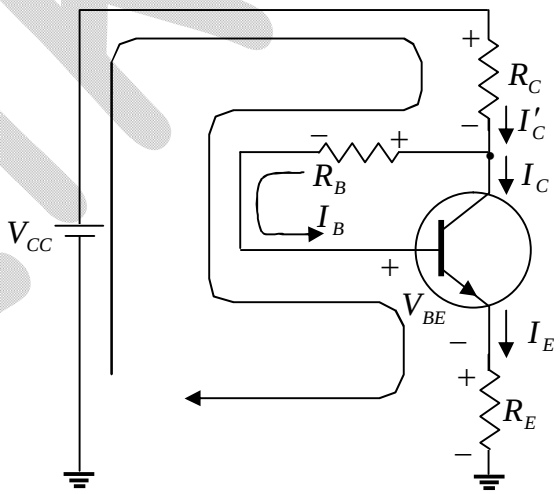


Figure 3.41: Base-emitter loop for the network of Figure 3.40.

In general, therefore, the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

In general, the equation for I_B had the following format: $I_B = \dfrac{V'}{R_B + \beta R'}$ with the absence of R' for the fixed-bias configuration, $R' = R_E$ for the emitter-bias setup (with $(\beta + 1) \cong \beta$), and $R' = R_C + R_E$ for the collector-feedback arrangement. The voltage V' is the difference between two voltage levels.

$$\Rightarrow I_{C_Q} = \frac{\beta V'}{R_B + \beta R'} \qquad \because I_C = \beta I_B$$

Collector-Emitter Loop

The collector-emitter loop for the network is provided in figure 3.42. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$-V_{CC} + I_C' R_C + V_{CE} + I_E R_E = 0$$

$$-V_{CC} + I_C (R_C + R_E) + V_{CE} = 0$$

$\because I_C' = I_C$ and $I_E = I_C$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

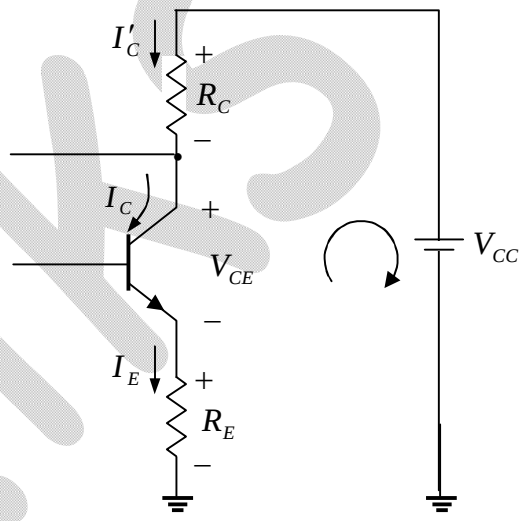


Figure 3.42: Collector-emitter loop for the network of figure 3.40.

3.8.2 Saturation Conditions

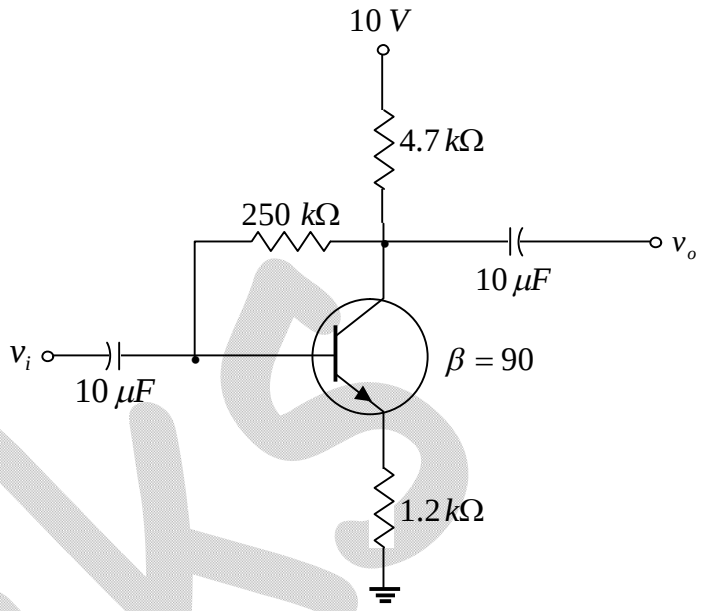
Using the approximation $I_C' = I_C$ the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$I_{C_{sat}} = I_{C_{\max}} = \frac{V_{CC}}{R_C + R_E}$$

3.8.3 Load-Line Analysis

Continuing with the approximation $I_C' = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} will be defined by the chosen bias configuration.

Example: Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of figure shown below.



Solution:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$I_B = \frac{10V - 0.7V}{250\ \ k\Omega + (90)(4.7\ \ k\Omega + 1.2\ \ k\Omega)}$$

$$I_B = \frac{9.3V}{25.\ \ k\Omega + 531\ \ k\Omega} = \frac{9.3V}{781\ \ k\Omega}$$

$$I_B = 11.91\ \mu A$$

$$I_{C_Q} = \beta I_B = (90)(11.91\mu A) = 1.07\ mA$$

$$\because V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$\Rightarrow V_{CE_Q} = 10 - (1.07mA)(4.7k\Omega + 1.2k\Omega) = 3.69\ V$$