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ELECTRONICS AND EXPERIMENTAL METHODS

(NET/JRF, GATE, JEST, TIFR)

ELECTRONICS AND EXPERIMENTAL METHODS CONTENT (PART-1 ANALOG ELECTRONICS)

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ELECTRONICS AND EXPERIMENTAL METHODS
(PART-2 DIGITAL ELECTRONICS & EXPERIMENTAL METHODS)

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CHAPTER-3
P-N JUNCTION DIODE

3.1 Semiconductor Diode

In an *n*-type material the electron is called the majority carrier and the hole the minority carrier. In an *p*-type material the holes are the majority carrier and the electrons are minority carrier.

If the two materials are "joined" the electrons and holes in the region of the junction will combine resulting in a lack of carriers in the region near the junction. This region of uncovered positive and negative ions is called the depletion region due to the depletion of mobile carriers in this region.

Since the diode is two terminal devices, the application of a voltage across its terminals leaves three possibilities: **no bias** $(V_D = 0V)$, **forward bias** $(V_D > 0V)$ and **reverse bias** $(V_D < 0V)$. Each is a condition that will result in a response that one must clearly understand if the device is to be applied effectively.

3.1.1 No Applied Bias $(V_D = 0V)$

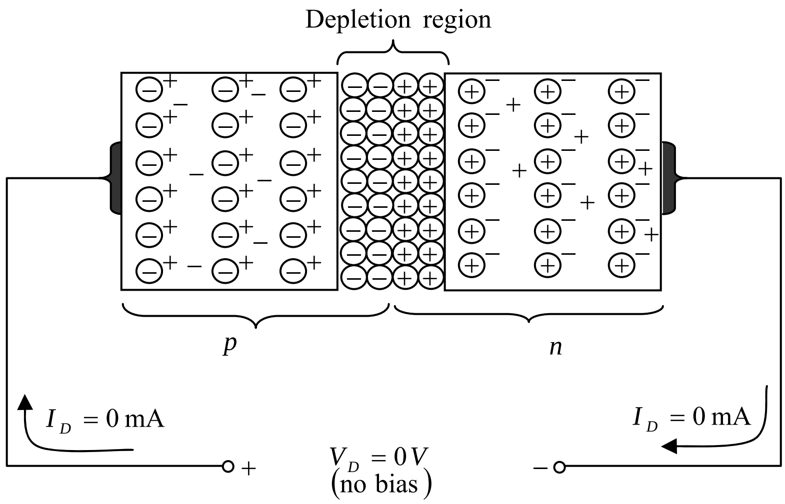

Figure 3.1: *p-n* junction with no applied bias.

Under no bias condition, any minority carriers (holes) in the *n*-type material that find themselves within the depletion region will pass directly into the *p*-type material. The closer the minority carrier is to the junction, the greater the attraction for the layer of negative ions and the less the opposition of the positive ions in the depletion region of the *n*-type material.

For further discussions we shall assume that all the minority carriers in the *n*-type material that find themselves in the depletion region due to their random motion will pass directly into the *p*-type material. Similar discussion can be applied to the minority carriers (electrons) of the *p*-type material.

The majority carriers (electrons) of the *n*-type material must overcome the attractive forces of the layer of positive ions in the *n*-type material and the shield of negative ions in the *p*-type material in order to migrate into the area beyond the depletion region of the *p*-type material. Again the same type of discussion can be applied to the majority carriers (holes) of the *p*-type material.

In the absence of an applied bias voltage, the net flow of charge in any one direction for a semiconductor diode is zero.

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3.1.2 Reverse Bias Condition $(V_D < 0V)$

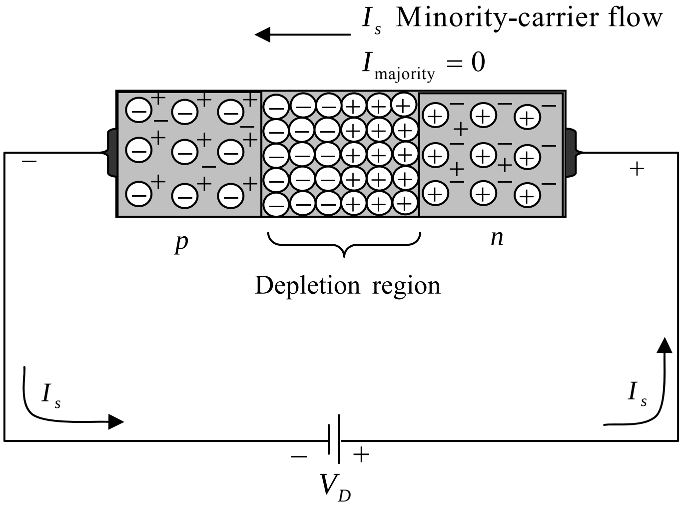


Figure 3.2: Reversed biased *p-n* junction.

If an external potential of *V* volts is applied across the *p-n* junction such that the positive terminal is connected to the *n*-type material and the negative terminal is connected to the *p*-type material, the number of uncovered positive ions in the depletion region of the *n*-type material will increase due to the large number of "free" electrons drawn to the positive potential of the applied voltage.

For similar reasons, the number of uncovered negative ions will increase in the *p*-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero.

The number of minority carriers, however, that find themselves entering the depletion region will not change, resulting in minority-carrier flow. *The current that exists under reverse bias conditions is called the reverse saturation current and is represented by* I_s or I_0.

3.1.3 Forward Bias Condition $(V_D > 0V)$

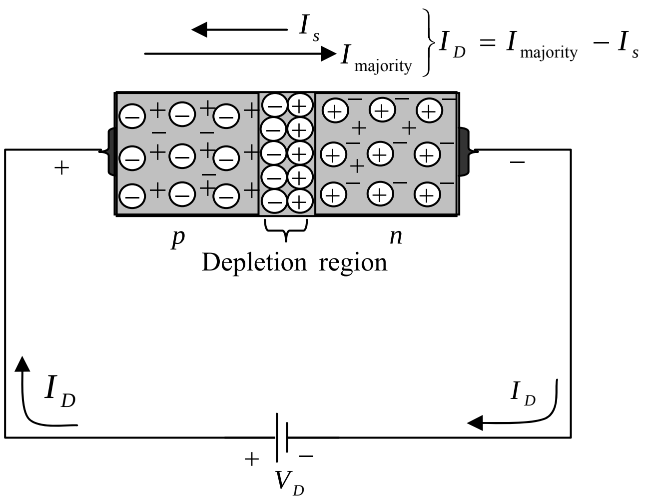


Figure 3.3: Forward biased *p-n* junction.

A forward-bias or "on" condition is established by applying the positive potential to the *p*-type material and the negative potential to the *n*-type material as shown in figure 3.3. Thus *a semiconductor diode is forward-biased when the association p-type positive and n-type negative has been established.*

The application of a forward-bias potential V_D will "pressure" electrons in the *n*-type material and holes in the *p*-type material to recombine with the ions near the boundary and reduce the width of the depletion region. The resulting minority-carrier flow of electrons from the *p*-type material to the *n*-type material (and of holes from the *n*-type material to the *p*-type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction.

An electron in the *n*-type material now "sees" a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the *p*-type material. As the applied bias increases in magnitude the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current as shown in the forward-bias region of the characteristics.

3.1.4 Ideal Diode

Before examining the construction and characteristics of an actual device, we first consider the ideal device, to provide a basis for comparison. The ideal diode is a two-terminal device having the symbol and characteristics shown in figure 2.4(a) and 2.4(b), respectively.

Ideally, a diode will conduct current in the direction defined by the arrow in the symbol and act like an open circuit to any attempt to establish current in the opposite direction. In essence: The characteristics of an ideal diode are those of a switch that can conduct current in only one direction.

The ideal diode, therefore, is a short circuit in the region of conduction and is an open circuit in the region of non conduction.

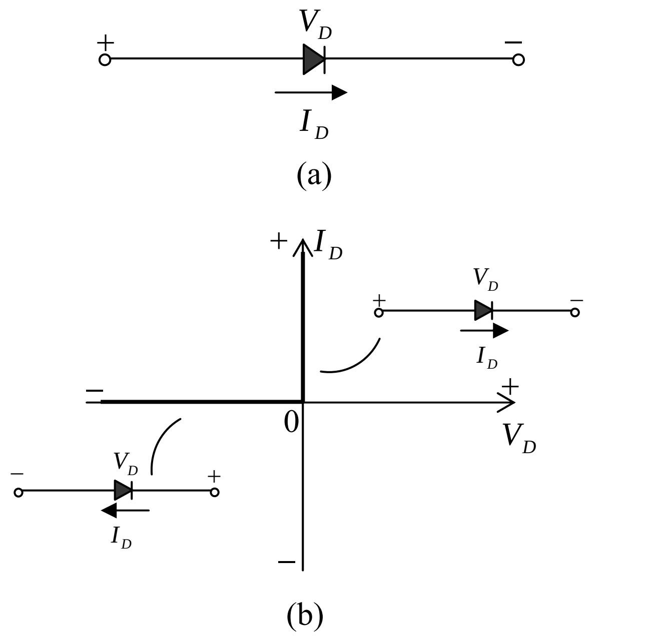


Figure 3.4: Ideal Diode: (a) Symbol; (b) Characteristics.

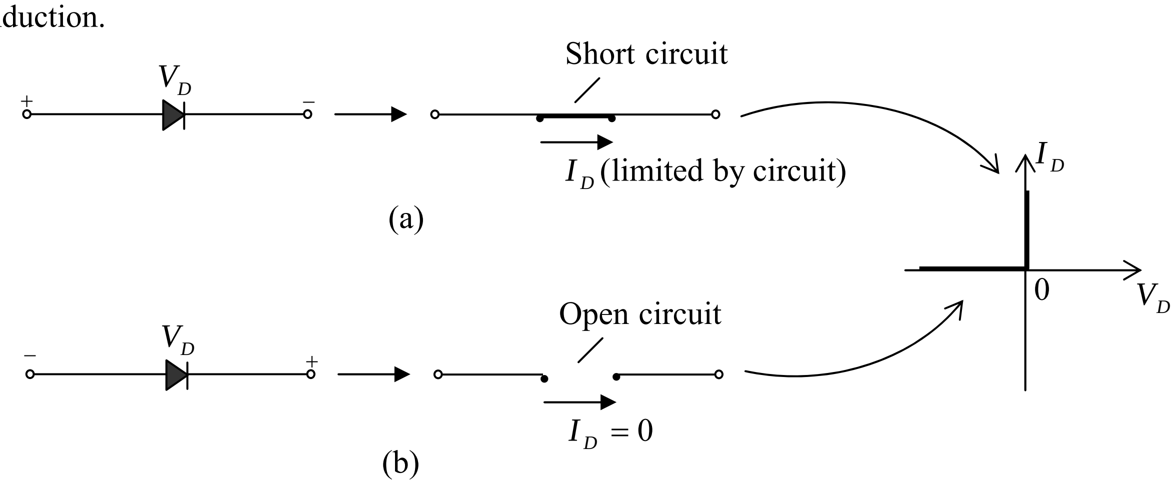


Figure 3.5: (a) Conduction and (b) non-conduction states of the ideal diode as determined by the applied bias.

3.1.5 Diode Characteristics ($V_\gamma = 0.7V$ for Si and $V_\gamma = 0.3V$ for Ge)

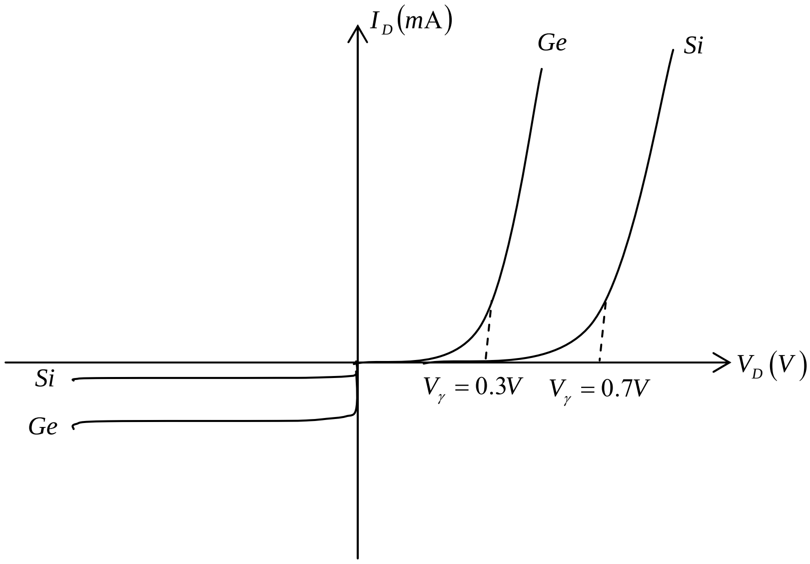


Figure 3.6: Comparison of *Si* and *Ge* semiconductor diodes.

It is clear from the characteristics of figure 3.6 that to forward bias the diode minimum voltage of V_γ is required. This voltage V_γ is called cut-in voltage of the diode. The closer the upward swing is to the vertical axis, the more "ideal" the device. However, the other characteristics of silicon as compared to germanium still make it the choice in the majority of commercially available units.

3.1.6 Diode Equation

$I_D = I_s\left(e^{V_D/\eta V_T} - 1\right)$ where I_s = reverse saturation current,

$V_T = \frac{kT}{e}$ is volt equivalent of temperature and $\eta = 1$ for Ge and $\eta = 2$ for Si devices.

Note:
The reverse saturation current in a germanium diode is normally larger by a factor of about 1000 than the reverse saturation current in a silicon diode of comparable ratings. I_s is in the range of μA for a Ge diode and nA for a silicon diode at room temperature.

Example: At $300K$, for a diode current of $1\ mA$, a certain germanium diode requires a forward bias of $0.1435V$, whereas a certain silicon diode requires a forward bias $0.718V$. Under the conditions stated above, find the closest approximation of the ratio of reserve saturation current in germanium diode to that in silicon diode.

Solution: $\eta = 1$ for Germanium

$\eta = 2$ for Silicon at low value of current

$$I = I_{O_{Si}}\left(e^{\frac{V_{D1}}{\eta V_T}} - 1\right) \ldots\ldots(\text{i}) \Rightarrow I = I_{O_{Ge}}\left(e^{\frac{V_{D2}}{\eta V_T}} - 1\right) \ldots\ldots(\text{ii})$$

L.H.S of (i) = (ii)

$$\Rightarrow I_{O_{Si}}\left(e^{\frac{V_{D1}}{\eta V_T}} - 1\right) = I_{O_{Ge}}\left(e^{\frac{V_{D2}}{\eta V_T}} - 1\right) \Rightarrow \frac{I_{O_{Ge}}}{I_{Osi}} = \frac{e^{\frac{V_{D1}}{\eta V_T}} - 1}{e^{\frac{V_{D2}}{\eta V_T}} - 1} = \frac{e^{\frac{0.718}{2\times26\times10^{-3}}} - 1}{e^{\frac{0.1435}{26\times10^{-3}}} - 1} = 4\times10^3$$

3.1.7 Breakdown Diodes

Diodes which are designed with adequate power-dissipation capabilities to operate in the breakdown region may be employed as voltage-reference or constant-voltage devices. Such diodes are known as avalanche, breakdown or Zener diodes. They are used characteristically in the manner indicated in the figure 3.7.

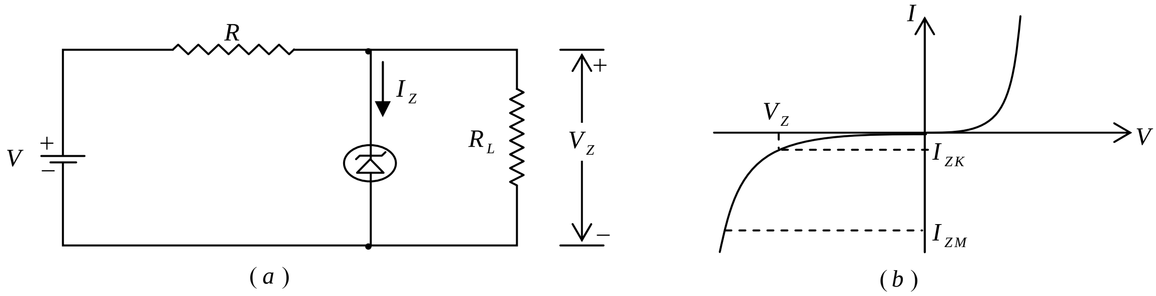


Figure 3.7: (a) Zener diode as voltage regulator (b) Zener charachteristics.

The source V and resistor R are selected so that initially, the diode is operating in the breakdown region. Here the diode voltage, which is also the voltage across the load R_L, is V_Z, and the diode current is I_Z. The diode will now regulate the load voltage against variations in load current and against variations in supply V, because in the break-down region only small changes in diode voltage produce large changes in diode current. Moreover, as load current or supply voltage changes, the diode current will accommodate itself to these changes to maintain a nearly constant load voltage.

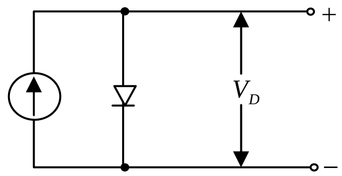
The diode will continue to regulate until the circuit operation requires the diode current to fall to I_{ZK}, in the neighborhood of the knee of the diode volt-ampere curve. The upper limit on diode current is determined by the power dissipation rating of the diode.

3.1.8 The Temperature Dependence of the V-I Characteristics

The volt-ampere relationship contains the temperature implicitly in the two symbols V_T and I_s. If the temperature is increased at a fixed voltage, the current increases. However if we now reduce V, then I may be brought back to its previous value. It is found that for either silicon or germanium (at room temperature) $\frac{dV}{dT} \approx -2.5 \, mV/{}^0C$ in order to maintain a constant value of I.

It should be noted that $\left|\frac{dV}{dT}\right|$ decreases with increasing T.

Example: In the figure, silicon diode is carrying a constant current of $1mA$. When the temperature of the diode is $20^0C, V_D$ is found to be $700mV$. If the temperature rises to 40^0C, then find the approximate value of V_D.



Solution: For either Si or Ge; $\frac{dV}{dT} \simeq -2.5mV/{}^0C$

In order to maintain a constant values of I

$$T_2 - T_1 = 40 - 20 = 20^0C$$

Change in V_D, $-2.5 \times 20mV = -50mV$

Therefore,

$$V_D = 700 - 50 = 650 \simeq 660mV$$

3.2 Diode Resistances

3.2.1 DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in figure 3.8 and applying the following equation:

$$R_D = \frac{V_D}{I_D}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant current source, the resistance determined will be at a preset current level (typically, a few milliamperes).

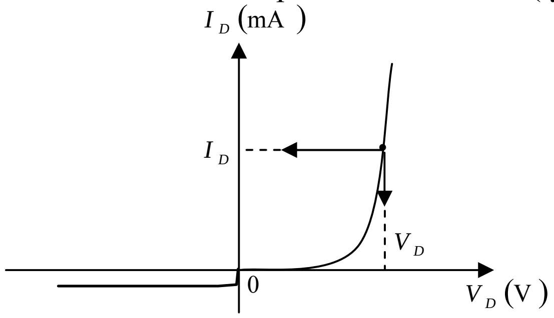


Figure 3.8: Determining the *dc* resistance of a diode at a particular operating point.

3.2.2 AC or Dynamic Resistance

The dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in figure 3.9(a). With no applied varying signal, the point of operation would be the *Q*-point appearing on figure determined by the applied dc levels. The designation *Q*-point is derived from the word quiescent which means "still or unvarying."

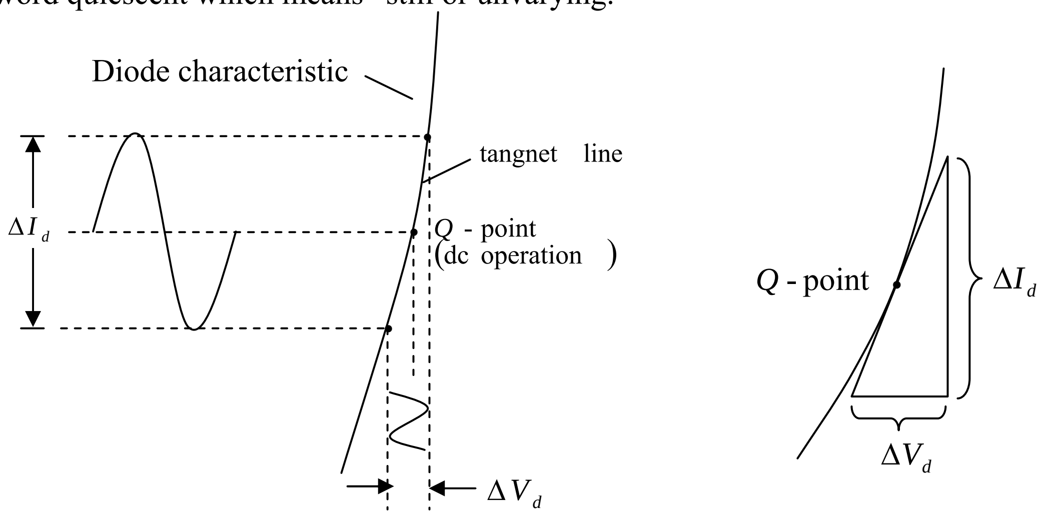


Figure 3.9: (a) Defining ac Resistance. (b) Determining the ac Resistance at a *Q*-point.

A straight line drawn tangent to the curve through the *Q*-point as shown in figure 3.9(b) will define a particular change in voltage and current that can be used to determine the *ac* or *dynamic* resistance for this region of the diode characteristics. An effort should be made to keep the change in voltage and current as small as possible and equidistant to either side of the *Q*-point.

In equation form $r_d = \frac{\Delta V_d}{\Delta I_d}$ where Δ signifies a finite change in the quantity.

For small-signal operation the dynamic resistance *r* is an important parameter and is defined as the reciprocal of the slope of the volt ampere characteristic $r \equiv \frac{dV}{dI}$.

The dynamic resistance is not a constant, but depends upon the operating voltage.

For a semiconductor diode, the dynamic conductance $g \equiv \frac{1}{r}$

$$g \equiv \frac{dI}{dV} = \frac{I_s e^{V/\eta V_T}}{\eta V_T} = \frac{I + I_s}{\eta V_T} \Rightarrow \boxed{r \approx \frac{\eta V_T}{I}} \quad \because I = I_s\left(e^{V/\eta V_T} - 1\right) \text{ and } \left|\frac{V}{\eta V_T}\right| >> 1,\ I >> I_S.$$

At room temperature, for η = 1, $r = \frac{26}{I}$, where *I* is in *mA* and *r* is in Ω. For a forward current of 26 *mA* the dynamic resistance is 1Ω.

3.3 Diode Capacitances

3.3.1 Space-Charge or Transition Capacitance

A reverse bias causes majority carriers to move away from the junction, thereby uncovering more immobile charges. Hence the thickness of the space charge layer at the junction increases with reverse voltage. The increase in uncovered charge with applied voltage may be considered a capacitive effect. We may define an incremental capacitance C_T by: $C_T = \left|\frac{dQ}{dV}\right|$ where *dQ* is the increase in charge caused by a change *dV* in voltage. It follows from this definition that a change in voltage *dV* in a time *dt* will result in a current $i = \frac{dQ}{dt}$ given by $i = C_T \frac{dV}{dt}$ where C_T is not a constant, but depends upon the magnitude of the reverse voltage. For a particular bias $C_T = \frac{\varepsilon A}{d}$, where A is cross sectional area, d is width of the depletion region and ε is permittivity of the medium.

3.3.2 Diffusion Capacitance

For a forward bias a capacitance which is much larger than the transition capacitance lies in the injected charge stored near the junction outside the transition region. It is convenient to introduce an incremental capacitance, defined as the rate of change of injected charge with voltage, called the diffusion or storage, capacitance C_D.

Charge control description of a diode

If the bias is in the forward direction, the potential barrier at the junction is lowered and holes from the *p*-side enter the *n*- side. Similarly electrons from the *n*-side move into the *p*-side. This process of minority-carrier injection has been discussed earlier. The excess hole density falls off exponentially with distance.

Assume that one side of the diode, say the *p* material, is so heavily doped in comparison with the *n* side that the current *I* is carried across the junction entirely by holes moving from the *p* to the *n* side or $I = I_{pn}(0)$. The excess minority charge *Q* will then exist only on the *n* side.

Now $I = \frac{Q}{\tau}$, where $\tau = \tau_p =$ mean life for holes.

The above equation states that the diode current (which consists of holes crossing the junction from the *p* to the *n* side) is proportional to the stored charge *Q* of excess minority carriers. The factor of proportionality is the reciprocal of the decay time constant (the mean lifetimeτ) of the minority carriers. Thus in the steady state, the current *I* supplies minority carriers at the rate at which these carriers are disappearing because of the process of recombination.

Static Derivation of C_D

Since, $I = \frac{Q}{\tau}$ and $C_D = \frac{dQ}{dV} = \tau \frac{dI}{dV} = \tau g = \frac{\tau}{r} = \frac{\tau I}{\eta V_T}$

where $g = \frac{dI}{dV}$ is the diode incremental conductance and $r = \frac{1}{g}$ is the diode incremental resistance.

We see that the diffusion capacitance is proportional to the current *I*. In the above derivation we have assumed that the diode current *I* is due to holes only. If this assumption is not satisfied then above equation gives the diffusion capacitance C_{D_p} due holes only and a similar expression can be obtained for the diffusion capacitance C_{D_n} due to electrons. The total diffusion capacitance can then be obtained as the sum of C_{D_p} and C_{D_n}.

Note: For a reverse bias, *g* is very small and C_D may be neglected compared with C_T.

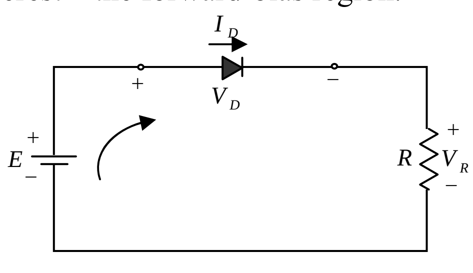
For a forward current, on the other hand, C_D is usually much larger than C_T.

Despite the large value of C_D, the time constant rC_D may not be excessive because the dynamic forward resistance $r = 1/g$ is small. Thus $rC_D = \tau$.

3.4 Load Line Analysis

The applied load will normally have an important impact on the point or region of operation of a device. If the analysis is performed in a graphical manner, a line can be drawn on the characteristics of the device that represents the applied load. The intersection of the load line with the characteristics will determine the point of operation of the system. Such an analysis is, for obvious reasons, called *load-line analysis*.

Consider the network of figure 3.10(a) employing a diode having the characteristics of figure 3.10(b). Note in figure 3.10(a) that the "pressure" established by the battery is to establish a current through the series circuit in the clockwise direction. The fact that this current and the defined direction of conduction of the diode are a "match" reveals that the diode is in the "on" state and conduction has been established. The resulting polarity across the diode will be as shown in figure 3.10(a) and the first quadrant (V_D and I_D positive) of figure 3.10 (b) will be the region of interest – the forward-bias region.



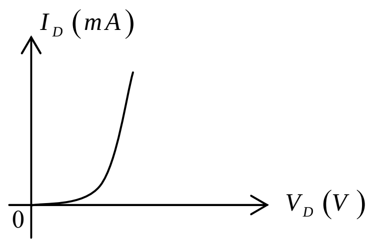


Figure 3.10: (a) Series diode configuration (b) Characteristics.

Applying Kirchhoff's voltage law to the series circuit of figure 3.10 (a) will result in

$$-E + V_D + V_R = 0 \Rightarrow E = V_D + V_R$$

$$\Rightarrow E = V_D + I_D R$$

The two variables of above equation (V_D and I_D) are the same as the diode axis variables of figure 3.10(a). This similarity permits a plotting of the equation on the same characteristics of figure 3.10 (b).

The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis $I_D = 0A$ and anywhere on the vertical axis $V_D = 0\ V$.

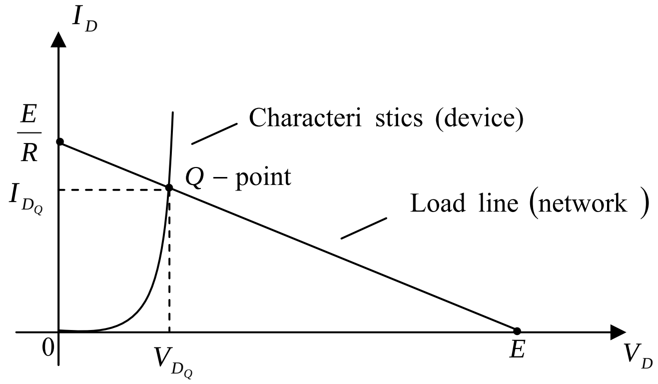


Figure 3.11: Drawing the load line and finding the point of operation.

If we set $V_D = 0\ V$ in equation $E = V_D + I_D R$ and solve for I_D, we have the magnitude of I_D on the vertical axis. Thus $E = V_D + I_D R = 0\ V + I_D R$ and $I_D = \left.\frac{E}{R}\right|_{V_D = 0V}$.

If we set $I_D = 0\ A$ in equation $E = V_D + I_D R$ and solve for V_D, we have the magnitude of V_D on the horizontal axis. Thus $E = V_D + (0A)R$ and $V_D = E|_{I_D = 0A}$.

A straight line drawn between the two points will define the load line as depicted in figure 3.11. Change the level of R (the load) and the intersection on the vertical axis will change. The result will be a change in the slope of the load line and a different point of intersection between the load line and the device characteristics.

We now have a load line defined by the network and a characteristics curve defined by the device. The point of intersection between the two is the point of operation for this circuit. By simply drawing a line down to the horizontal axis the diode voltage V_{D_Q} can be determined, whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{D_Q}.

The current I_D is actually the current through the entire series configuration of figure 3.10(a). The point of operation is usually called the *quiescent point* (abbreviated "Q-point") to reflect its "still, unmoving" qualities as defined by a dc network.

The solution obtained at the intersection of the two curves is the same that would be obtained by a simultaneous mathematical solution of equations $E = V_D + I_D R$ and $I_D = I_s\left(e^{V_D/\eta V_T} - 1\right)$.

3.5 Series Diode Configurations with DC Inputs

In this section the approximate model is utilized to investigate a number of series diode configurations with dc inputs. The procedure described can, in fact, be applied to networks with any number of diodes in a variety of configurations.

For each configuration the state of each diode must first be determined. Which diodes are "on" and which are "off"? Once determined, the appropriate equivalent can be substituted and the remaining parameters of the network determined.

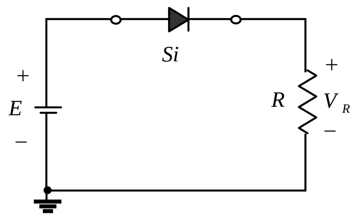
In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D \geq 0.7\ V$ for silicon and $V_D \geq 0.3\ V$ for germanium.

For each configuration, mentally replace the diodes with resistive elements and note the resulting direction as established by the applied voltages ("pressure"). If the resulting direction is a "match" with the arrow in the diode symbol, conduction above is, of course, contingent on the supply having a voltage greater than the "turn-on" voltage (V_γ) of each diode.

If a diode is in the "on" state, one can either place a 0.7 V drop across the element, or the network can be redrawn with the V_γ equivalent circuit. In time the preference will probably simply be to include the 0.7 V drop across each "on" diode and draw a line through each diode in the "off" or open state. Initially, however, the substitution method will be utilized to ensure that the proper voltage and current levels are determined.

The series circuit of figure 3.12(a) will be used to demonstrate the approach described in the paragraphs above. The state of the diode is first determined by mentally replacing the diode with a resistive element as shown in figure 3.12(b). The resulting direction of I is a match with the arrow in the diode symbol and since $E > V_\gamma$ the diode is in the "on" state.

The network is then redrawn as shown in figure 3.12(c) with the appropriate equivalent model for the forward-biased silicon diode. Note for future reference that the polarity of V_D is the same as would result if in fact the diode were a resistive element.



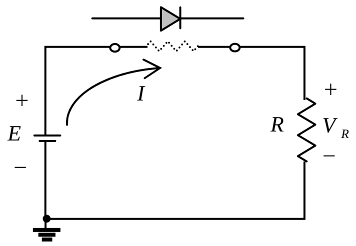


Figure 3.12: (a) Series diode (b) Determining the state of the diode of figure

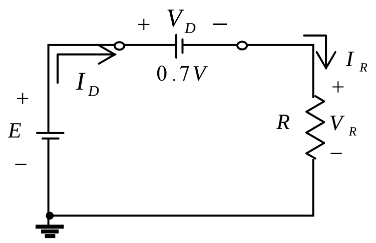
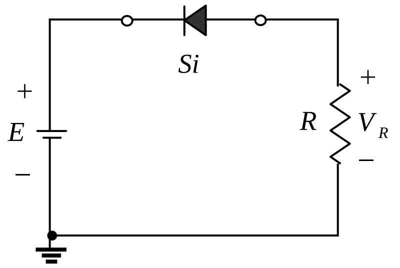


Figure 3.12: (c) Substituting the equivalent model for the "on" diode of figure (a).

The resulting voltage and current levels are the following.

$$V_D = V_\gamma, \; V_R = E - V_\gamma \; \text{ and } I_D = I_R = \frac{V_R}{R}.$$

In figure 2.13(a) the diode of figure 2.12(a) has been reversed. Mentally replacing the diode with a resistive element as shown in figure 2.13(b) will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of figure 2.13(c). Due to the open circuit, the diode current is 0 A and the voltage across



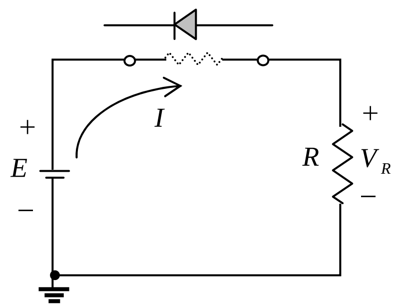


Figure 3.13: (a) Reversing the diode of figure 3.12(a).

(b) Determining the state of diode of figure (a).

the resistor *R* is the following:

$$V_R = I_R R = I_D R = 0V$$

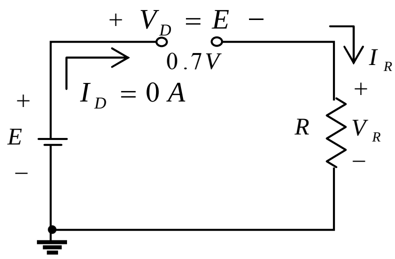
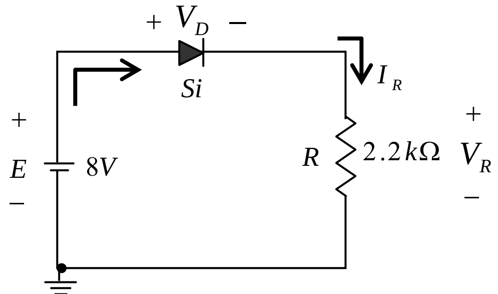


Figure 3.13(c): Substituting the equivalent model for the "off" diode of figure

The fact that $V_R = 0V$ will establish *E* volts across the open circuit as defined by Kirchhoff's voltage law. *Always keep in mind that under any circumstances–dc, ac instantaneous values, pulses, and so on – Kirchhoff's voltage law must be satisfied!*

Example: For the series diode configuration of figure shown below, determine V_D, V_R, and I_D.



Solution: Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state.

$V_D = 0.7\ V$, $V_R = E - V_D = 8\ V - 0.7\ V = 7.3\ V$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3V}{2.2k\Omega} \cong 3.32\ mA$$

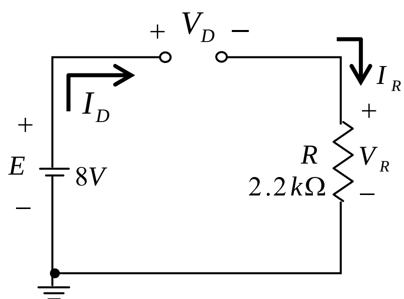
Example: Repeat above example with the diode reversed.

Solution: Removing the diode, we find that the direction of *I* is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of figure shown below, where $I_D = 0\ A$ due to the open circuit. Since $V_R = I_R R$, $V_R = (0)\ R = 0\ V$.

Applying Kirchhoff's voltage law around the closed loop yields

$-E + V_D + V_R = 0$

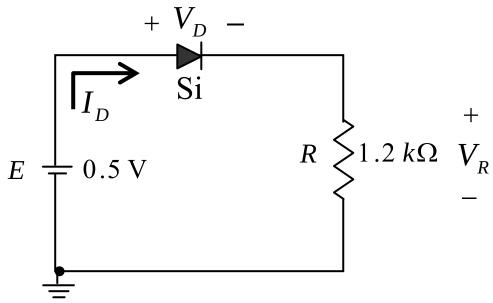
and $\quad V_D = E - V_R = E - 0 = E = 8\ V$



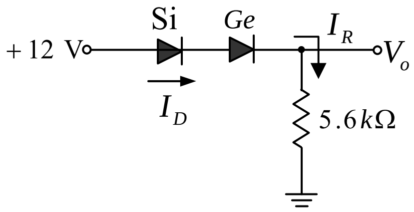
Example: For the series diode configuration of figure shown below, determine V_D, V_R, and I_D.

Solution: Although the "pressure" establishes a current with the same direction as the arrow symbol the level of applied voltage is insufficient to turn the silicon diode "on". The resulting voltage and current levels are therefore the following:

$I_D = 0\ A$, $V_R = I_R R = I_D R = (0\ A)\ 1.2\ k\Omega = 0\ V$ and $V_D = E = 0.5\ V$



Example: Determine V_0 and I_D for the series circuit of figure shown below.



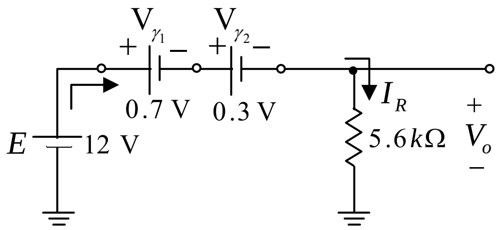
Solution: The resulting current has the same direction as the arrowheads of the symbols of both diodes, and the network of figure shown below results because

$E = 12V > (0.7\ V + 0.3\ V) = 1\ V$.

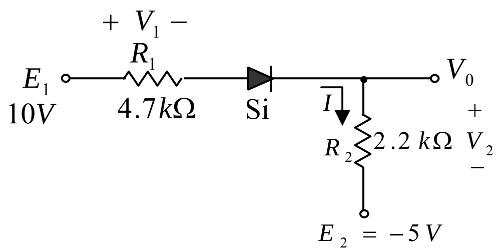
Note the redrawn supply of 12 V and the polarity of V_0 across the 5.6 $k\Omega$ resistor. The resulting voltage

$V_0 = E - V_{\gamma_1} - V_{\gamma_2} = 12V - 0.7V - 0.3V = 11V$

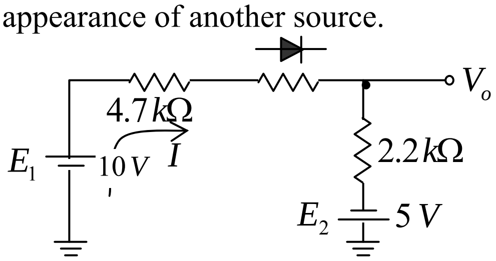
and $I_D = I_R = \dfrac{V_R}{R} = \dfrac{V_0}{R} = \dfrac{11V}{5.6k\Omega} \cong 1.96mA$

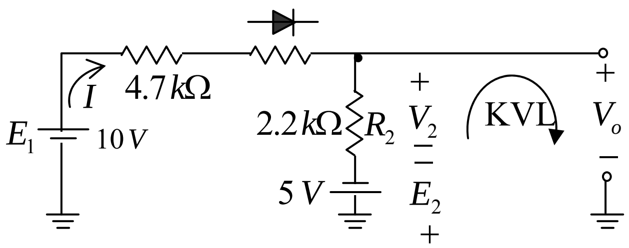


Example: Determine I, V_1, V_2 and V_0 for the series dc configuration of figure shown below.



Solution: The sources are drawn and the current direction indicated as shown in figure below. Note that the "on" state is noted simply by the additional V_D= 0.7 V on the figure. This eliminates the need to redraw the network and avoids any confusion that may result from the appearance of another source.





The resulting current through the circuit is,

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10V + 5V - 0.7V}{4.74k\Omega + 2.2k\Omega} = \frac{14.3V}{6.9k\Omega} \cong 2.07mA$$

and the voltages are $\quad V_1 = IR_1 = (2.07\ mA)\ (4.7\ k\Omega) = 9.73\ V$

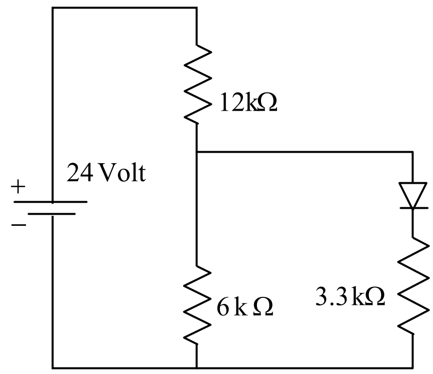
$V_2 = IR_2 = (2.07\ mA)\ (2.2\ k\Omega) = 4.55\ V$

Applying Kirchhoff's voltage law to the output section in the clockwise direction will result in

$+E_2 - V_2 + V_0 = 0$ and $V_0 = V_2 - E_2 = 4.55\ V - 5\ V = -0.45\ V$.

The minus sign indicates that V_0 has a polarity opposite to that appearing in figure.

Example: In the following circuit, the voltage drop across the diode in forward bias condition is $0.7\,V$. Find the current passing through the $6k\Omega$ resistance.



Solution:

Let current through $12\,k\Omega$ is I and through diode is I_D

Then $\quad 0.7 + I_D \times 3.3 = (I - I_D) \times 6 \qquad (1)$

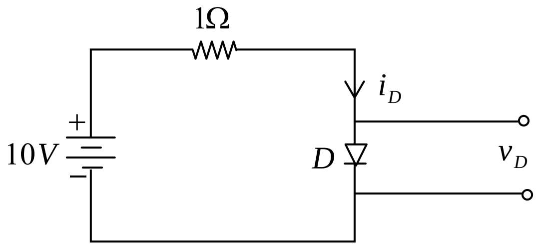
and $-24 + I \times 12 + (I - I_D) \times 6 = 0 \qquad (2)$

From (1) and (2)

$$I_D \approx 1mA.,\ I \approx \frac{5}{3}mA. \Rightarrow I - I_D \approx \frac{2}{3}mA \approx 0.7mA.$$

Example: A diode D as shown in the circuit has an i-v relation that can be approximated by

$$i_D = \begin{cases} v_D^2 + 2v_D, & \text{for } v_D > 0 \\ 0, & \text{for } v_D \le 0 \end{cases}$$



Find the value of i_D in the circuit.

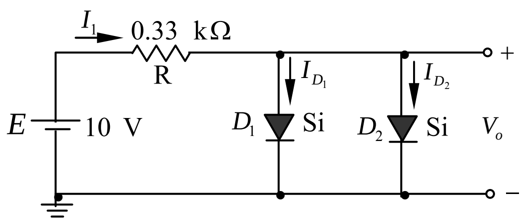
Solution:

$$-10 + (v_D^2 + 2v_D) \times 1 + v_D = 0 \Rightarrow v_D = 2V \Rightarrow i_D = 8\ A$$

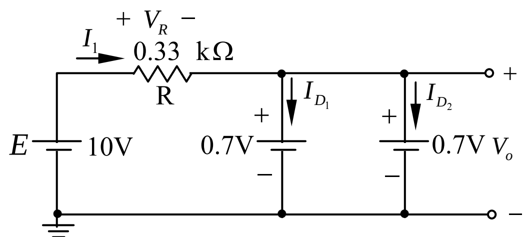
3.6 Parallel and Series–Parallel Configurations

The methods applied in series configurations can be extended to the analysis of parallel and series-parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

Example: Determine V_0, I_1, I_{D_1} and I_{D_2} for the parallel diode configuration as shown in figure.



Solution: For the applied voltage the "pressure" of the source is to establish a current through each diode in the same direction as shown in figure below. Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always the same and $V_0 = 0.7\ V$.

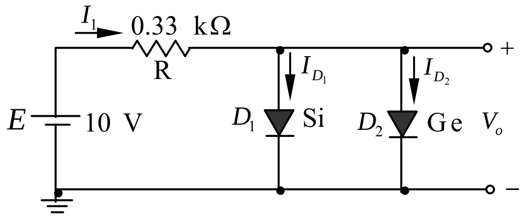


The current

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10V - 0.7V}{0.33k\Omega} = 28.18\,mA$$

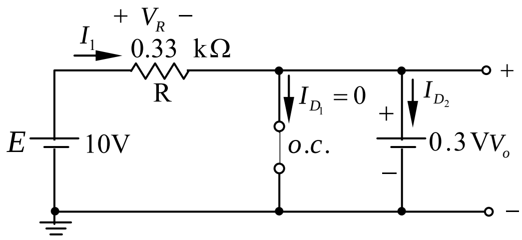
Assuming diodes of similar characteristics, $I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\,mA}{2} = 14.09\,mA$

Example: Determine V_0, I_1, I_{D_1} and I_{D_2} for the parallel diode configuration as shown in figure.

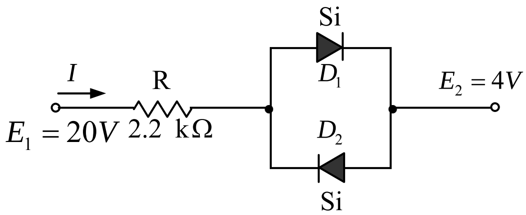


Solution: In this circuit diode D_2 is Ge diode. So once switch is ON, Ge diode will be ON and Si will be open circuited. Thus $V_0 = 0.3V$, $I_{D_1} = 0$ and

$$I_1 = I_{D_2} = \frac{10V - 0.3V}{0.33k\Omega} = 29.39\,mA$$



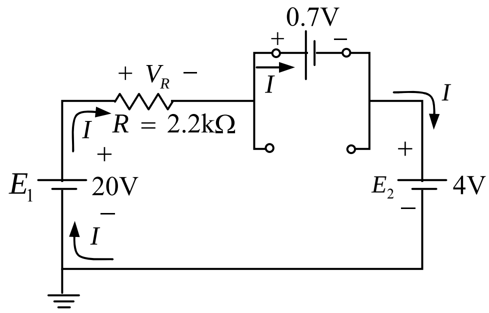
Example: Determine the current I for the network shown in figure below.



Solution:

Redrawing the network as shown in figure reveals that the resulting current direction is such as to turn on diode D_1 and turn off diode D_2. The resulting current I is then

$$I = \frac{E_1 - E_2 - V_D}{R} = \frac{20V - 4V - 0.7V}{2.2k\Omega} \cong 6.95\,mA$$



3b. PN JUNCTION DIODE APPLICATIONS

3.7 Rectifiers

3.7.1 Half-Wave Rectification

This circuit will generate a waveform v_o that will have an average value of particular use in the ac-to-dc conversion process.

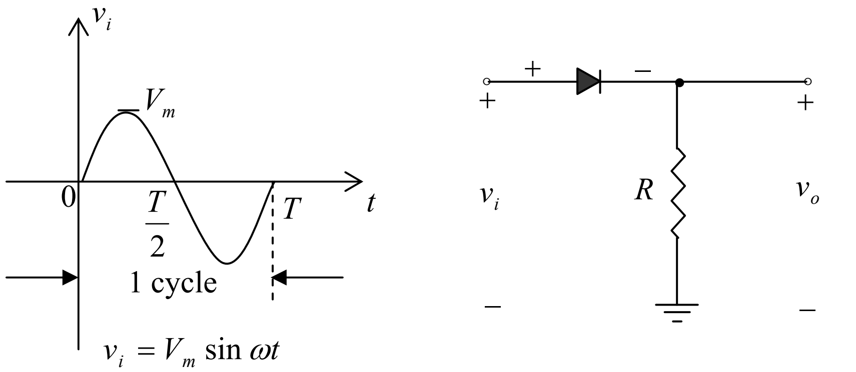


Figure 3.14: Half-Wave Rectification.

During the interval $t = 0 \rightarrow T/2$ the polarity of the applied voltage is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit shown in figure 3.15, where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode.

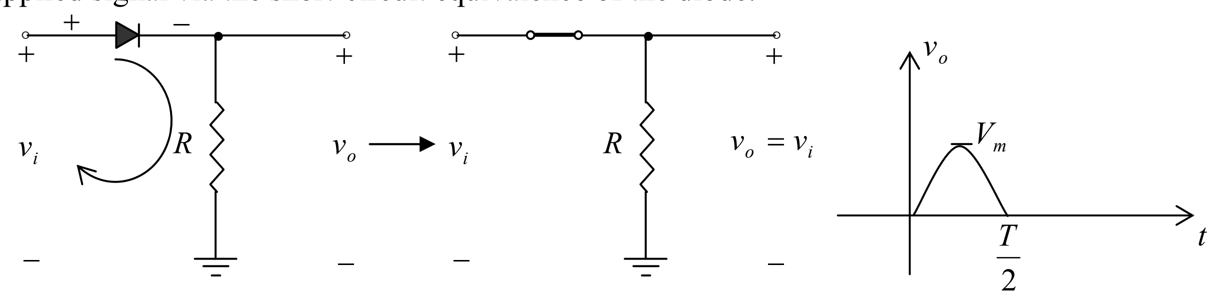


Figure 3.15: Conduction region ($0 \rightarrow T/2$).

For the period $t = T/2 \rightarrow T$, the polarity of input v_i is shown in figure 3.16 and the resulting polarity across the ideal diode produces an "off" state with an open circuit equivalent. The result is the absence of a path for charge to flow and $v_0 = 0V$ for the period $T/2 \rightarrow T$.

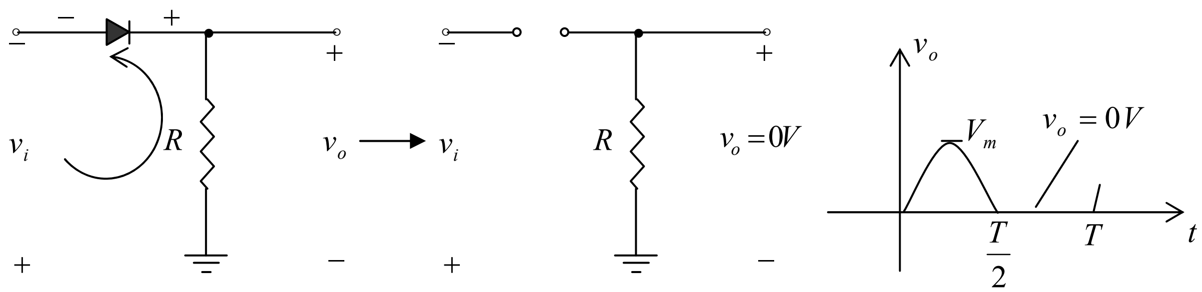


Figure 3.16: Nonconduction region ($T/2 \rightarrow T$).

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The process of removing one-half the input signal to establish a dc level is aptly called half-wave rectification.

The input v_i and the output v_0 were sketched together in figure 3.17 for comparison purposes.

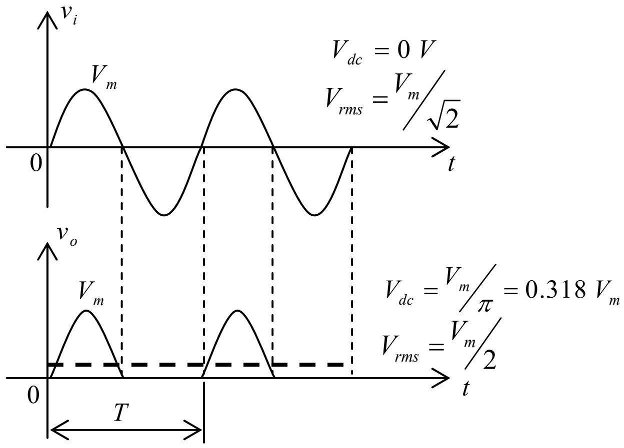

Figure 3.17: Half-wave rectified signal.

The process of removing one-half the input signal to establish a dc level is aptly called *half-wave rectification.*

We can find the average and rms value of any ac signal using relation

$$V_{dc} = \frac{1}{T}\int_0^T v\,d\theta \quad \text{and} \quad V_{rms} = \left(\frac{1}{T}\int_0^T v^2 d\theta\right)^{1/2}$$

where T is period of ac signal and v is instantaneous value of ac signal.

The output signal v_0 now has a net positive area above the axis over a full period and an average value determined by

$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} V_m \sin\theta d\theta = \frac{1}{2\pi}\int_0^{\pi} V_m \sin\theta d\theta = \frac{V_m}{\pi} = 0.318V_m$$

and $$V_{rms} = \left(\frac{1}{T}\int_0^T v^2 d\theta\right)^{1/2} = \left(\frac{1}{2\pi}\int_0^{2\pi} V_m^2 \sin^2\theta d\theta\right)^{1/2} = \left(\frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2\theta d\theta\right)^{1/2} = \frac{V_m}{2}$$

NOTE:

The effect of using a silicon diode with $V_\gamma = 0.7V$ is demonstrated in figure 3.18 for the forward-bias region. The applied signal must now be at least $0.7V$ before the diode can turn "on." For levels of v_i less than $0.7V$ the diode is still in an open-circuit state and $v_o = 0V$. When conducting, the difference between v_o and v_i is a fixed level of $V_\gamma = 0.7V$ and $v_0 = v_i - V_\gamma$. The net effect is a reduction in area above the axis, which naturally reduces the resulting dc voltage level. For situations where $V_m >> V_\gamma$ equation given below can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_\gamma)$$

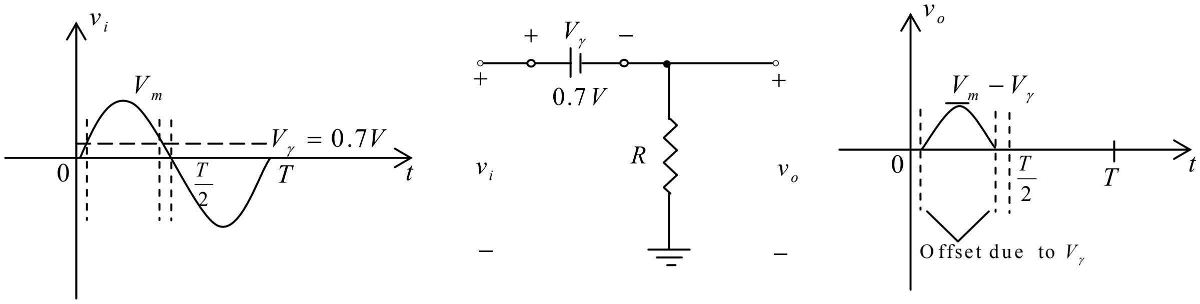

Figure 3.18: Effect of V_γ on half-wave rectified signal.

Peak Inverse Voltage (PIV) or Peak Reverse Voltage (PRV)

It is the voltage rating that must not be exceeded in the reverse-bias region. The required PIV rating for the half-wave rectifier can be determined from figure 3.19, which displays the reverse-biased diode with maximum applied voltage. Applying Kirchhoff's voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore, PIV rating $\geq V_m$

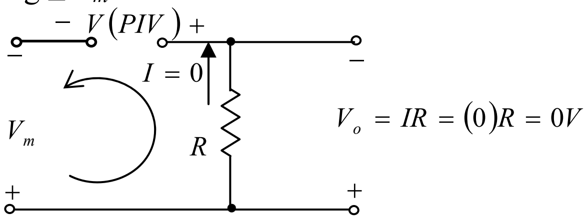

Figure 3.19: Determining the required PIV rating for the half-wave rectifier.

3.7.2 Full Wave Rectification

(i) Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification.* The most familiar network for performing such function appears in figure 3.20 with its four diodes in a bridge configuration.

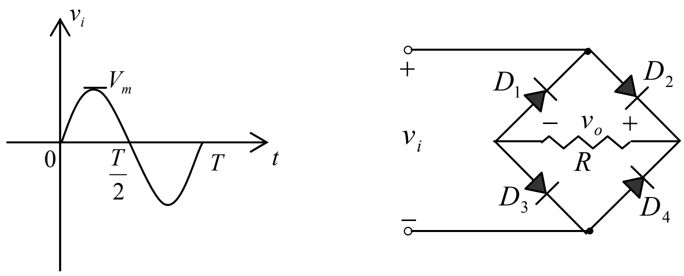

Figure 3.20: Full-wave bridge rectifier.

During period $t = 0 \rightarrow T/2$ the polarity of the input is shown in figure 3.21. The resulting polarities across the ideal diodes are shown to reveal that D_2 and D_3 are conducting while D_1 and D_4 are in the "off" state.

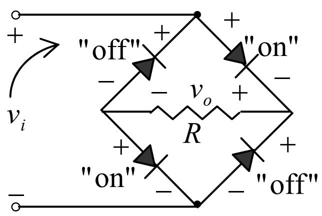

Figure 3.21: FWR for the period $0 \rightarrow T/2$ of the input voltage v_i.

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The net result is the configuration of figure 3.22, with its indicated current and polarity across R. Since the diodes are ideal the load voltage $v_0 = v_i$.

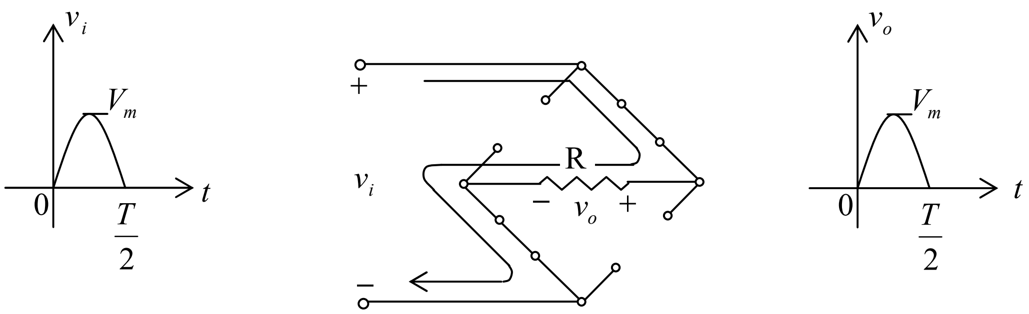

Figure 3.22: Conduction path for the positive region of v_i .

For the negative region of the input the conducting diodes are D_1 and D_4, resulting in the configuration of figure 3.23. The important result is that the polarity across the load resistor R is the same as during positive half cycle.

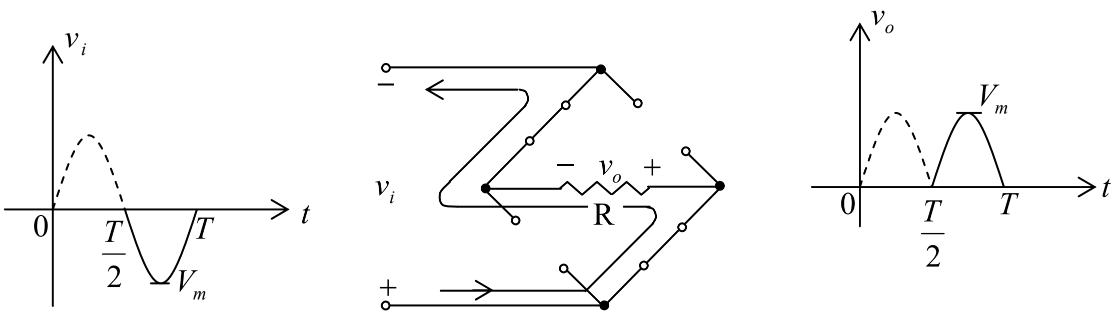

Figure 3.23: Conduction path for the negative region of v_i .

Over one full cycle the input and output voltages will appear as shown in figure 3.24.

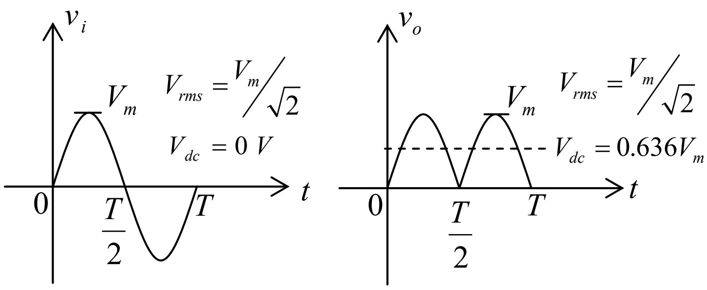

Figure 3.24: Input and output waveforms for a full-wave rectifier.

The output signal v_0 now has a net positive area above the axis over a full period and an average value determined by

$$V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_m \sin\theta d\theta = \frac{1}{\pi}\int_0^{\pi} V_m \sin\theta d\theta = \frac{2V_m}{\pi} = 0.636\ V_m$$

and $$V_{rms} = \left(\frac{1}{T}\int_0^{T} v^2 d\theta\right)^{1/2} = \left(\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2\theta d\theta\right)^{1/2} = \left(\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2\theta d\theta\right)^{1/2} = \frac{V_m}{\sqrt{2}}$$

Since the area above the axis for one full cycle is now twice that obtained for half-wave system, the dc level has also been doubled and $V_{dc} = \frac{2V_m}{\pi} = 0.636 V_m$.

NOTE: If silicon rather than ideal diodes are employed as shown in figure 3.25, an application of Kirchhoff's voltage law around the conduction path would result in

$$-v_i + V_\gamma + v_o + V_\gamma = 0 \text{ And } v_o = v_i - 2V_\gamma$$

The peak value of the output voltage v_0 is therefore $V_{0_{\max}} = V_m - 2V_\gamma$

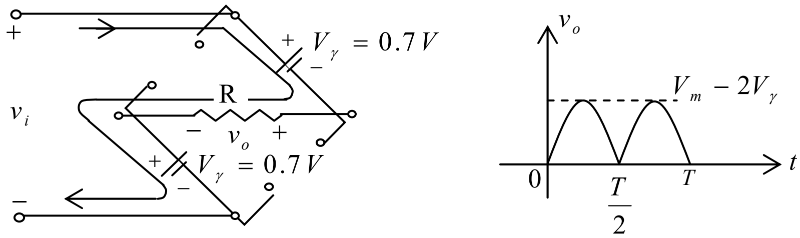

Figure 3.25: Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.

For situations where $V_m >> 2V_\gamma$ equation given below can be applied to determine the average value with a relatively high level of accuracy. $V_{dc} \cong 0.636(V_m - 2V_\gamma)$

PIV: The required PIV of each diode (ideal) can be determined from figure 3.26 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V_m and the PIV rating is defined by PIV $\geq V_m$

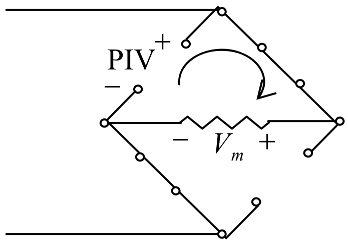

Figure 3.26: Determining the required PIV rating for the bridge configurations.

(ii) Center-Tapped transformer

A second popular full-wave rectifier appears in figure 3.27 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signals across each section of the secondary of the transformer.

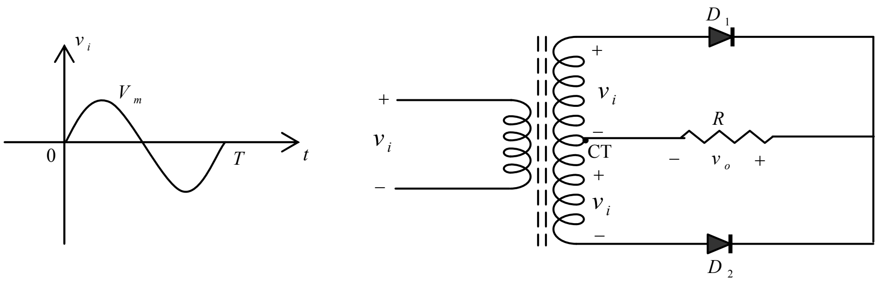

Figure 3.27: Centre-tapped transformer full-wave rectifier.

During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in figure 3.28. D_1 assumes the short-circuit equivalent and D_2 the open circuit equivalent as detrmined by the secondary voltages and the resulting current directions.The output voltage v_0 appears as shown in figure 3.28.

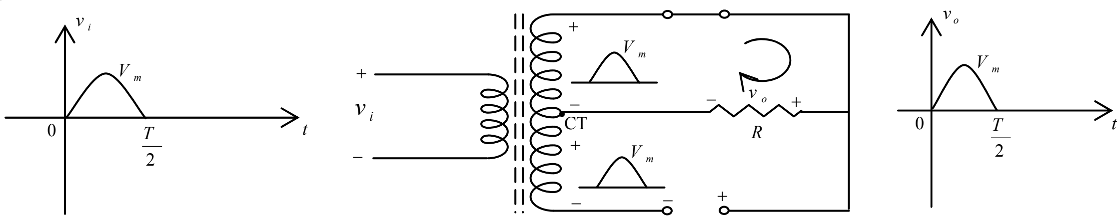

Figure 3.28: Network conditions for the positive region

During the negative portion of the input the network appears as shown in figure 3.29, reversing the roles of the diodes but maintaining the same polarity for the voltage across the load resistor R. The net effect is the same output as that appearing in positive half cycle with the same dc levels.

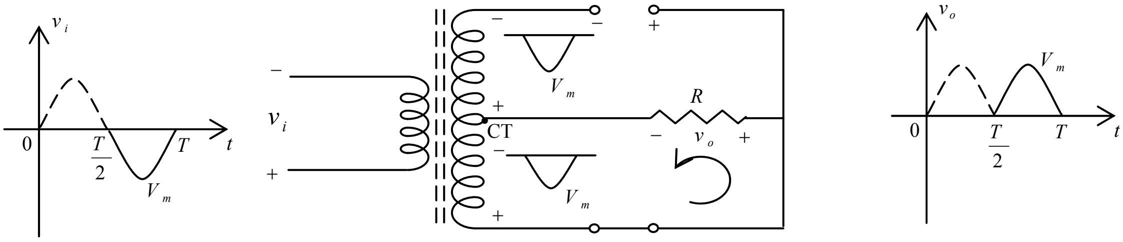

Figure 3.29: Network conditions for the negative region of v_i.

PIV: The network of figure 3.30 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop will result in

$$\text{PIV} = V_{\text{secondary}} + V_R \quad = V_m + V_m \quad \text{and} \qquad \text{PIV} \geq 2V_m .$$

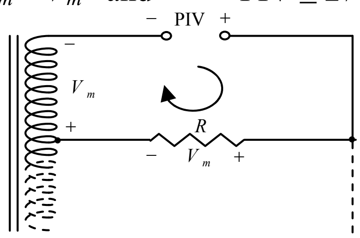

Figure 3.30: Determining the PIV level for the

3.8 Clippers

There are a variety of diode networks called clippers that have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform. The half-wave rectifier is an example of the simplest form of diode clipper– one resistor and diode. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

3.8.1 Series Clippers (Positive and Negative)

The response of the series configuration of figure 3.31(a) to a variety of alternating waveforms is provided in figure 3.31(b). Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper.

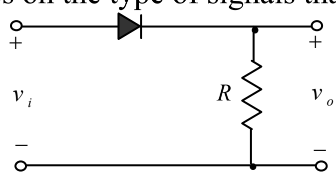

Figure 3.31(a): Series clipper.

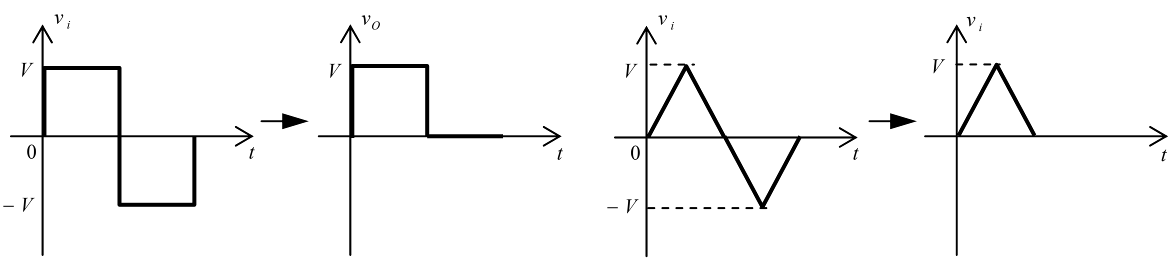

Figure 3.31(b): Input and output waveforms.

The addition of dc supply such as shown in figure 3.32 can have a pronounced effect on the output of a clipper. Our initial discussion will be limited to ideal diodes and the effect of V_γ will be discussed later.

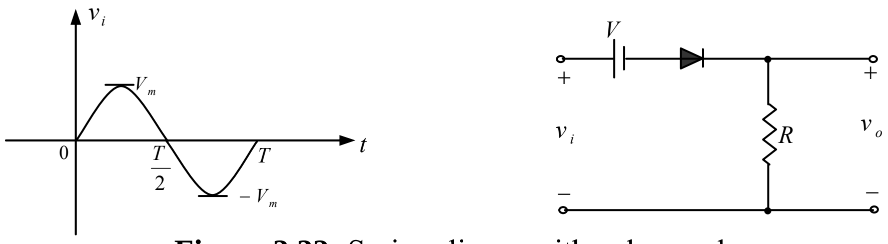

Figure 3.32: Series clipper with a dc supply.

There is no general procedure for analyzing above networks, but there are a few thoughts to keep in mind before analyzing these circuits.

1. *Make a mental sketch of the response of the network based on the direction of the diode and the applied voltage levels.*

The direction of the diode suggests that the signal v_i must be positive to turn it on. The dc supply further requires that the voltage v_i be greater than V volts to turn the diode on. The negative region of the input signal is "pressuring" the diode into the "off" state, supported further by the dc supply. In general, therefore, we can be quite sure that the diode is an open circuit ("off" state) for the negative region of the input signal.

2. *Determine the applied voltage (transition voltage) that will cause change in state for the diode.*

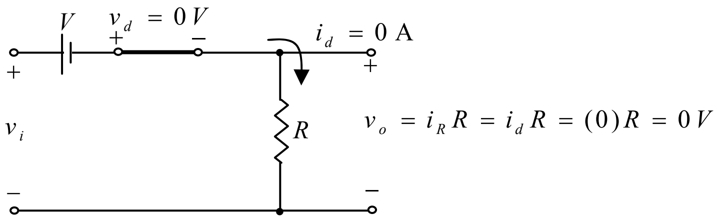

Figure 3.33: Determining the transition level.

For the ideal diode the transition between states will occur at the point on the characteristic where $v_d = 0V$ and $i_d = 0A$. Applying the condition $i_d = 0A$ at $v_d = 0$ will result in the configuration of figure 3.33, where it is recognized that the level of v_i that will cause a transition in state is: $v_i = V$.

For an input voltage greater than V volts the diode is in the short-circuit state, while for input voltage less than V volts it is in the open-circuit or "off" state.

3. *Be continually aware of the defined terminals and polarity of v_o.*

When the diode is in the short-circuit state such as shown in figure 3.34, the output voltage v_o can be determined by applying Kirchhoff's voltage law in the clockwise direction.

$-v_i + V + v_o = 0$ and $v_o = v_i - V$.

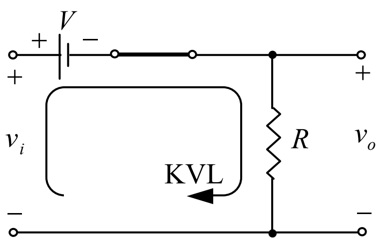

Figure 3.34: Determining v_o.

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4. *It can be helpful to sketch the input signal above the output and determine the output at instantaneous values of the input.*

It is then possible that the output voltage can be sketched from the resulting data points of v_o as demonstrated in figure 3.35.

Keep in mind that at an instantaneous value of v_i the input can be treated as a dc supply of that value and the corresponding dc value (the instantaneous value) of the output determined. For instance, at $v_i = V_m$ the network to be analyzed appears in figure 3.36.

For $V_m > V$ the diode is in the short-circuit state and $v_o = V_m - V$. At $v_i = V$ the diodes change state and at $v_i = -V_m$, $v_o = 0V$ and the complete curve for v_o can be sketched as shown in figure 3.37.

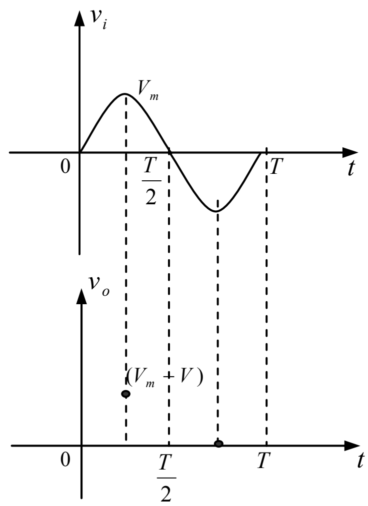


Figure 3.35: Determining levels

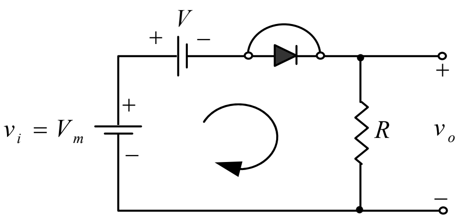


Figure 3.36: Determining v_o

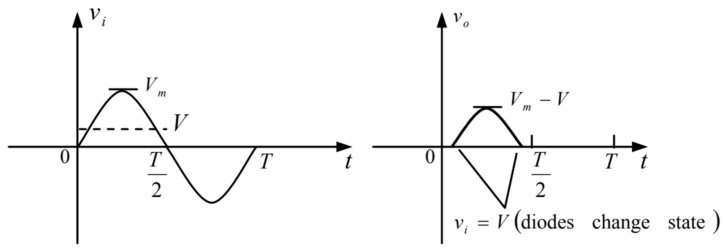
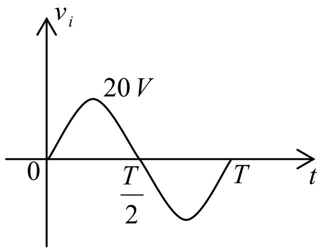
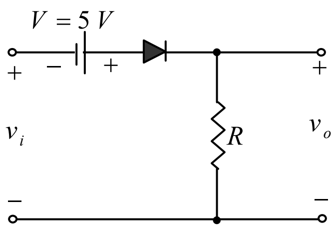


Figure 3.37:

Example: Determine the output waveform for the network shown in figure below.





Solution: The diode will be in "on" state for the positive region of v_i, especially when we note the aiding effect of V= 5V. The network will then appear as shown in figure (a) and $v_0 = v_i + 5V$. Substituting $i_d = 0$ at $v_d = 0$ for the transition levels, we obtain the network of figure (b) and $v_i = -5V$.

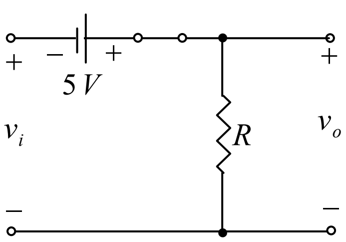


Figure (a): v_0 with diode in the "on" state.

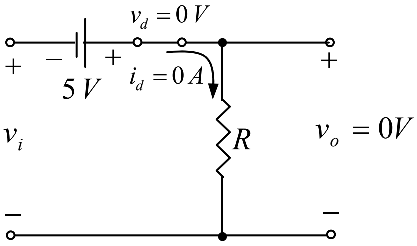


Figure (b): Determining the transition level.

For v_i more negative than $-5V$ the diode will enter its open-circuit state, while for voltages more positive than $-5V$ the diode is in the short-circuit state. The input and output voltage appear in figure shown below.

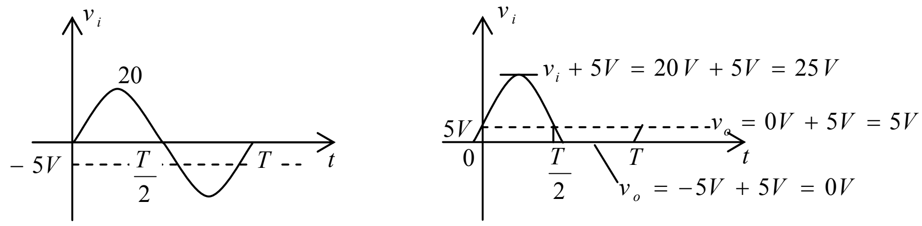
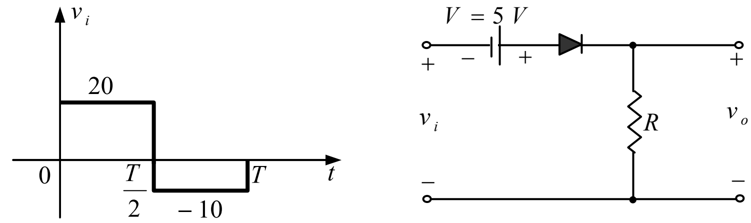


Figure:

Example: Repeat above example for the square-wave input shown in figure below.



Solution: For $v_i = 20V\ (0 \rightarrow T/2)$ the network of figure (a) will result. The diode is in the short-circuit state and $v_o = 20V + 5V = 25V$. For $v_i = -10V$ the network of figure (b) will result, placing the diode in the "off" state and $v_o = i_R R = 0 \times R = 0V$. The resulting output voltage appears in figure (c).

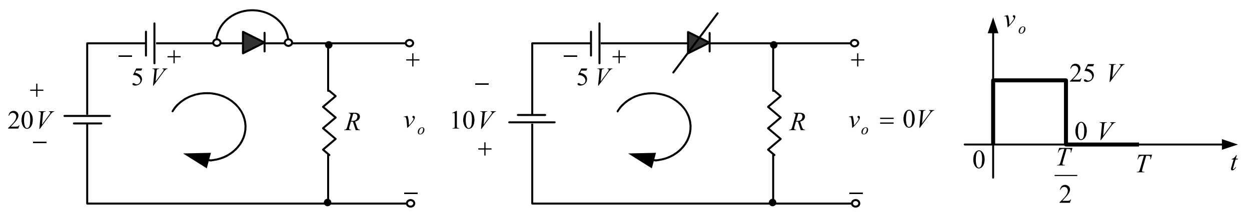


Figure (a): v_o at $v_i = 20V$ **Figure (b):** v_o at $v_i = -10V$ **Figure(c):**

3.8.2 Parallel Clippers (Positive and Negative)

The network of figure 3.38 is the simplest of parallel diode configurations with the output for the same inputs. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

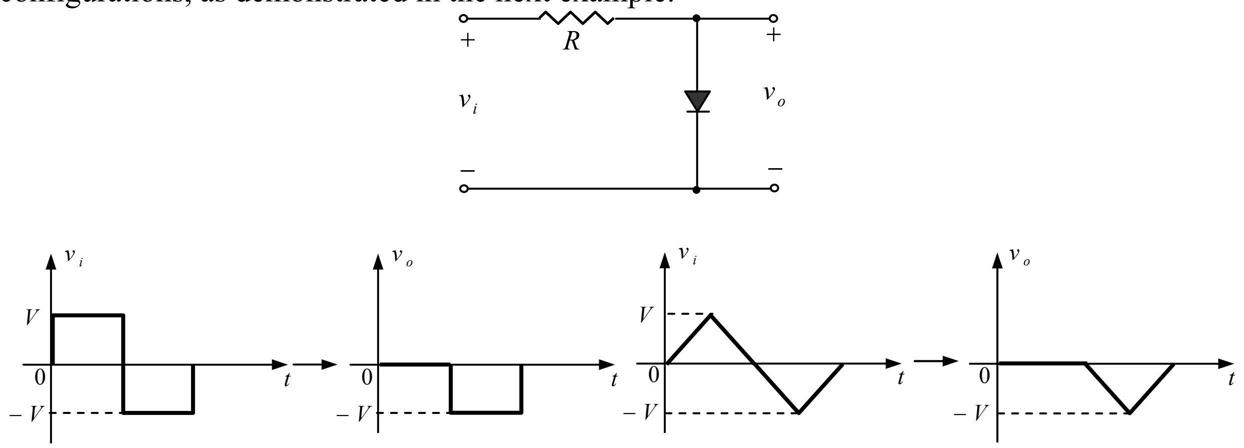
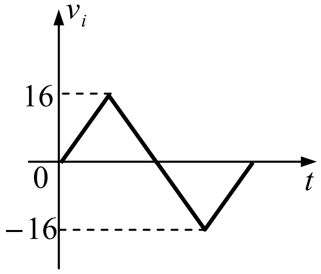
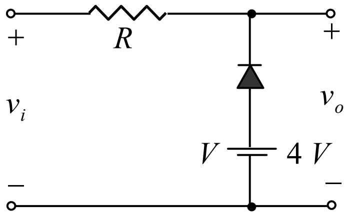


Figure 3.38: Response to a parallel clipper.

Example: Determine v_0 for the network of figure shown below.





Solution: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for the negative region of the input signal. For this region the network will appear as shown in figure below where the defined terminals for v_0 require that $v_0 = V = 4V$.

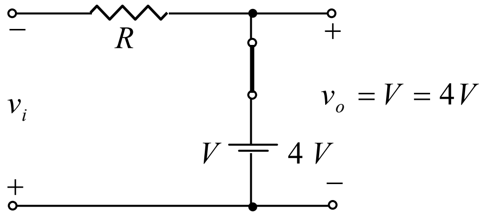


Figure: v_0 for the negative region of v_i.

The transition state can be determined from figure shown below, where the condition $i_d = 0A$ at $v_d = 0V$ has been imposed. The result is v_i (transition) $= V = 4\ V$.

Since the dc supply is obviously "pressuring" the diode to stay in the short-circuit state, the input voltage must be greater than 4 V for the diode to be in the "off" state. Any input voltage less than 4V will result in a short-circuited diode.

For the open-circuit state the network will appear as shown in figure below, where $v_0 = v_i$ .Completing the sketch of v_0 results in the waveform of figure shown below.

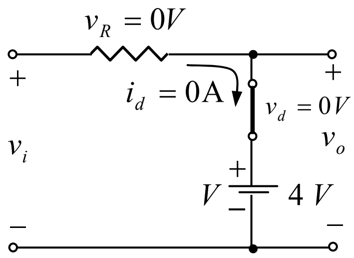


Figure: Determining the transition level.

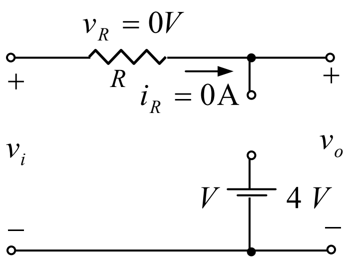


Figure: Determining v_0 for the open state of the diode

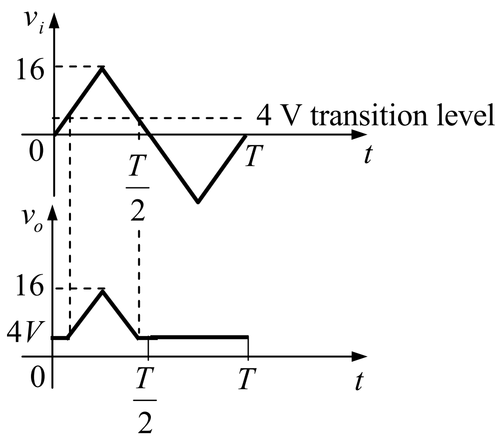


Figure: Sketching v_0 .

To examine the effect of V_γ on the output voltage, the next example will specify a silicon diode rather than an ideal diode equivalent.

Example: Repeat above example using a silicon diode with $V_\gamma = 0.7\ V$.

Solution: The transition voltage can first be determined by applying the condition $i_d = 0A$ at $v_d = 0.7V$ and obtaining the network of figure shown below. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$-v_i - V_\gamma + V = 0$$

and $v_i = V - V_\gamma = 4 - 0.7 = 3.3V$

$$v_R = i_d R = 0 \times R = 0V$$

For input voltages greater than 3.3V, the diode will be an open circuit and $v_0 = v_i$. For input voltages of less than 3.3 V, the diode will be in the "on" state and the network of figure shown below results, where $v_0 = 3.3V$.

Note that the only effect of V_γ was to drop the transition level to 3.3 V from 4 V.

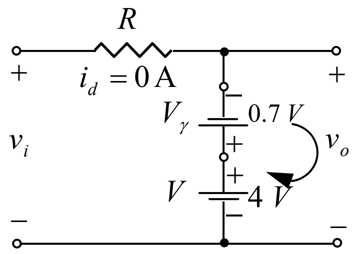


Figure: Determining the transition level.

There is no question that including the effects of V_γ was to drop the transition level to 3.3 V from 4V.

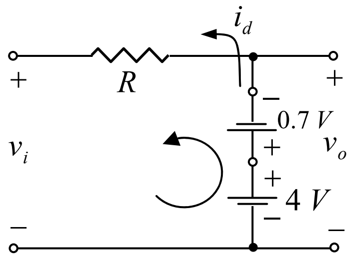


Figure: Determining v_o for the diode of figure 2.83 in the "on" state.

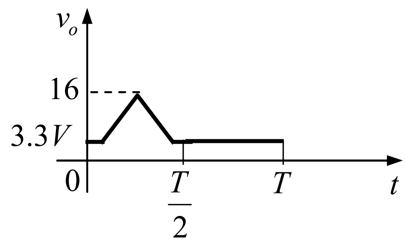


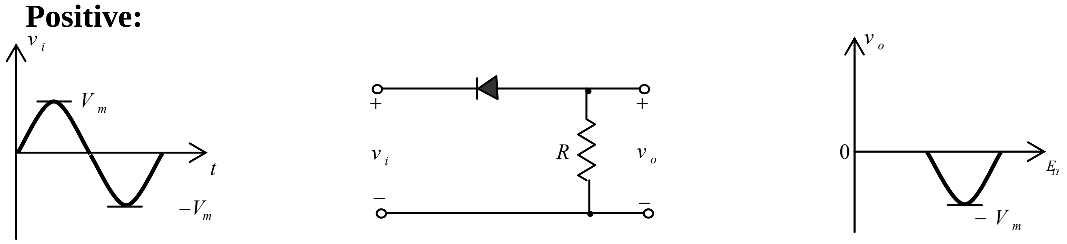
Figure: Sketching v_0.

Summary Clippers Networks

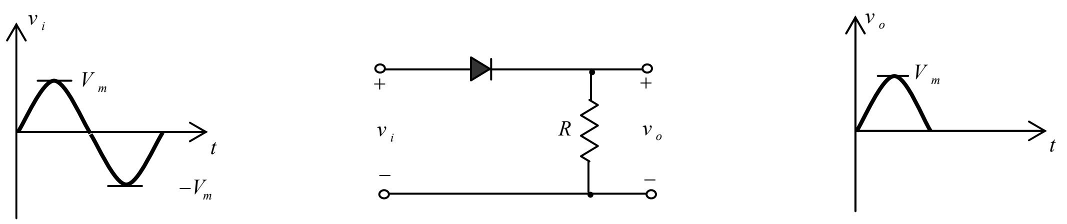
A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in figures shown below. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

Simple Series Clippers (Ideal Diodes)

Positive:

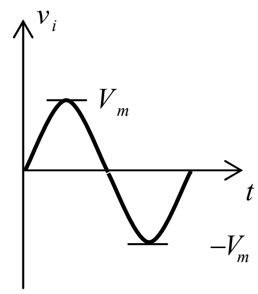


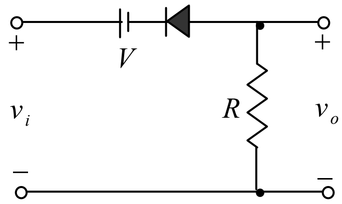
Negative:

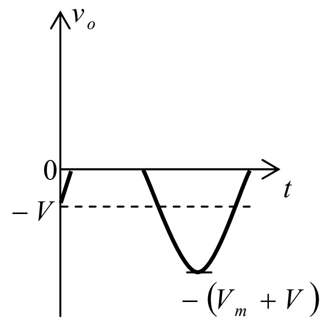


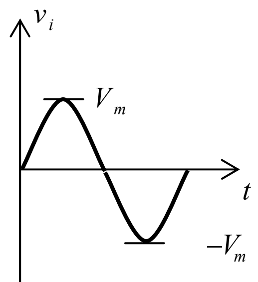
Biased Series Clippers (Ideal Diodes)

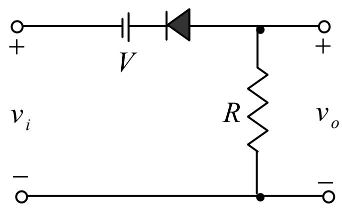
Positive:

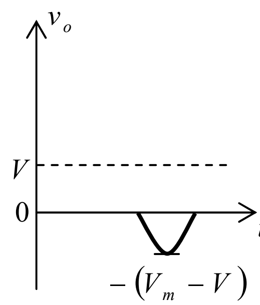




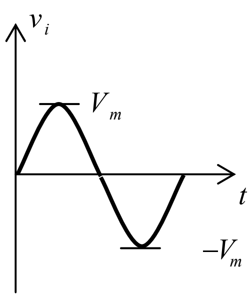


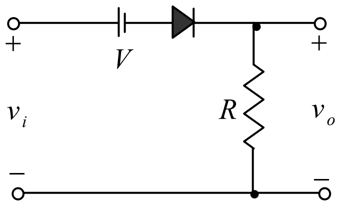


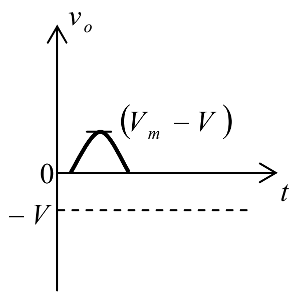


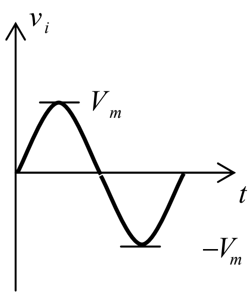


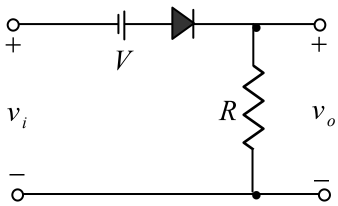
Negative

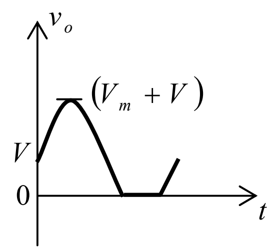






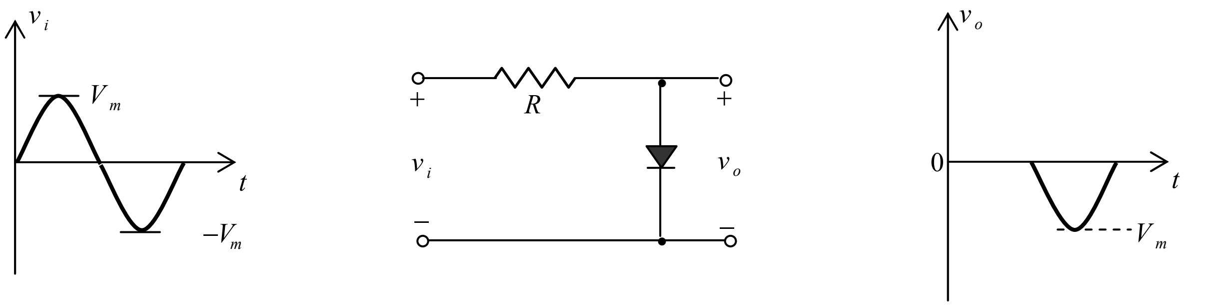




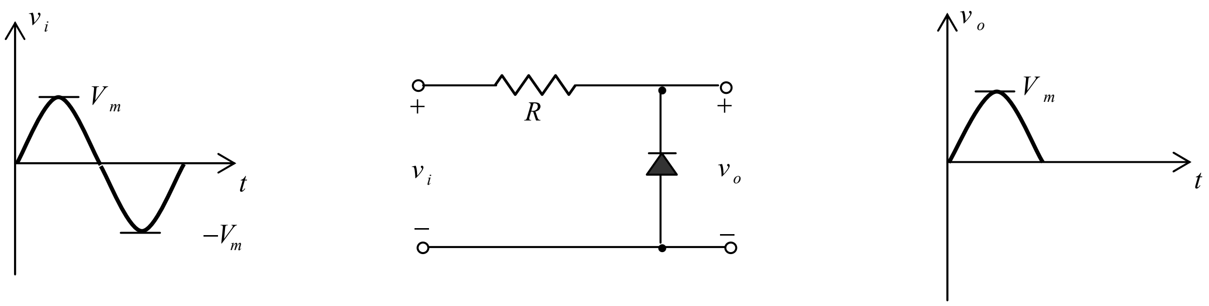


Simple Parallel Clippers (Ideal Diodes)

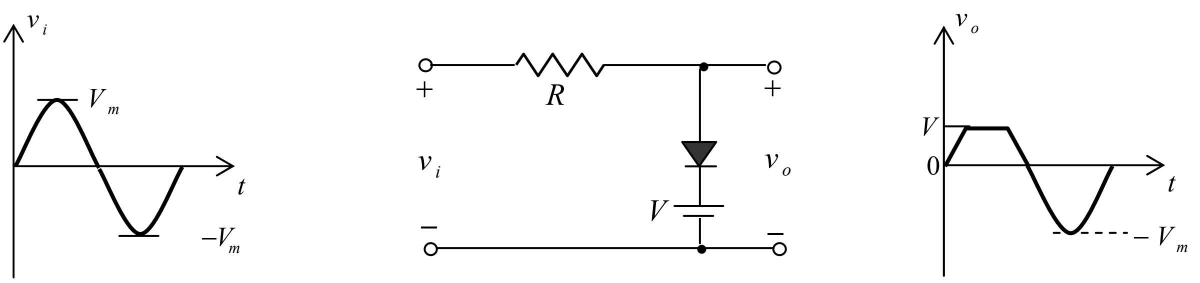
Positive:

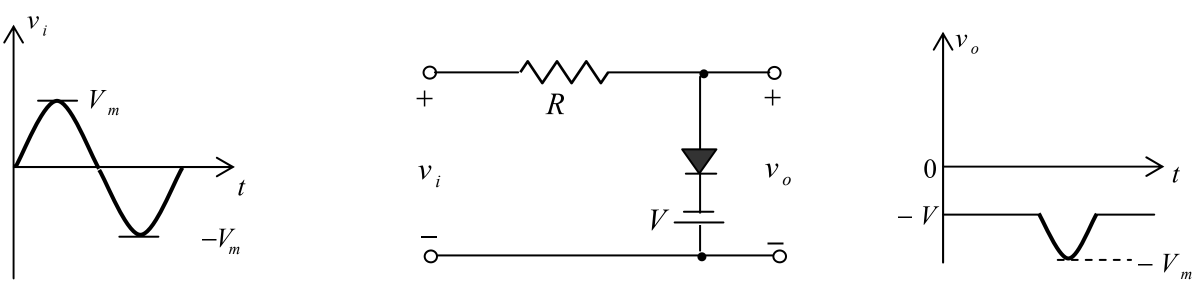


Negative:



Biased Parallel Clippers (Ideal Diodes)





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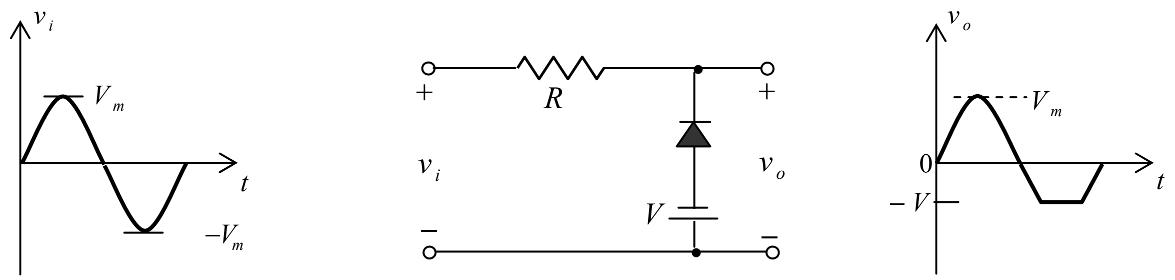
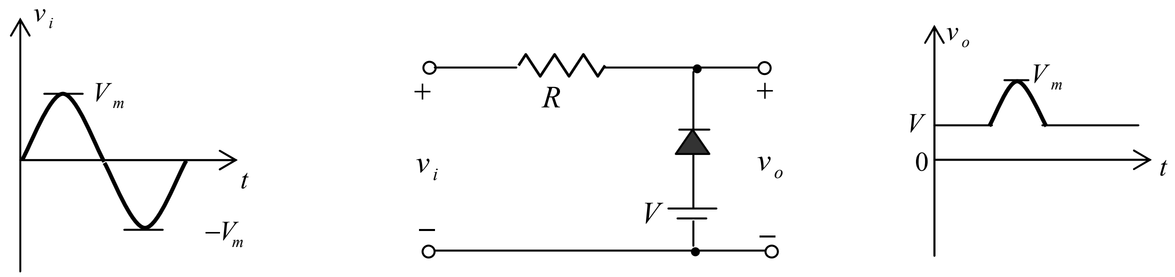
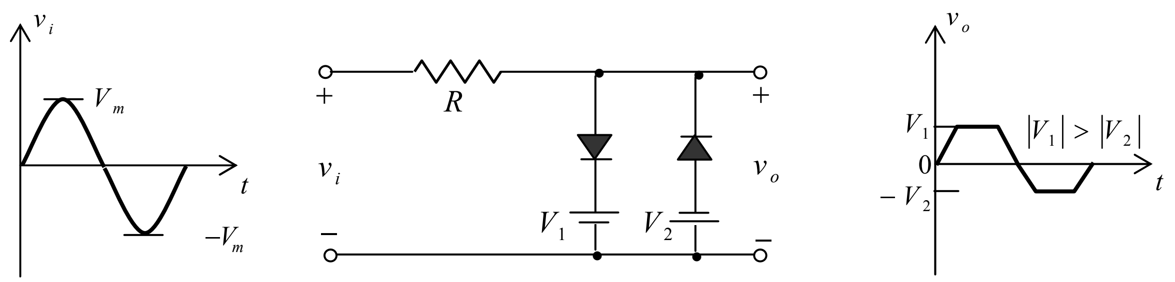
Negative:

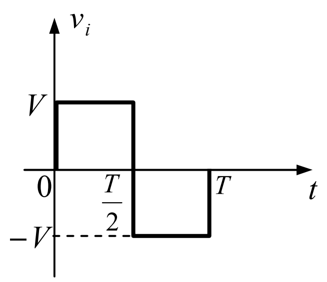




Miscellaneous



3.9 Clampers



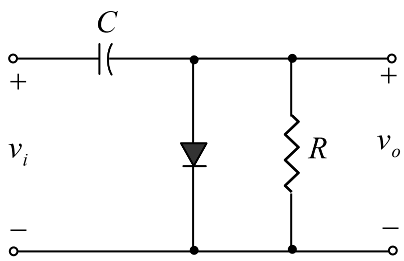


Figure 3.39: Clamper.

The *clamping* network is one that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the ***time constant*** $\tau = RC$ ***is large enough*** to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non-conducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants.

The network of figure 3.39 will clamp the input signal to the zero level (for ideal diodes).

During the interval $0 \rightarrow T/2$ the network will appear as shown in figure 3.40, with the diode in the "on" state effectively "shorting out" the effect of resistor R. The resulting RC time constant is so small (R is determined by the inherent resistance of the network) that the capacitor will charge to V volts very quickly. During this interval the output voltage is directly across the short circuit and $v_o = 0\ V$.

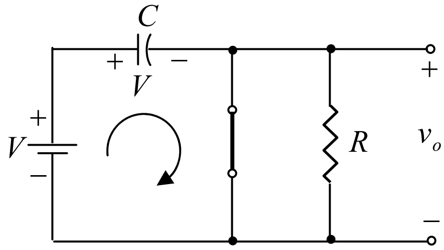


Figure 3.40: Diode "on" and the capacitor charging to V volts.

When the input switches to $-V$ state, the network will appear as shown in figure 3.41, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor-both "pressuring" current through the diode from cathode to anode.

Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ much greater than the period $T/2 \rightarrow T$ and it can be assumed on an approximate basis that the capacitor holds onto all its charge and therefore voltage (since $V = Q/C$) during this period.

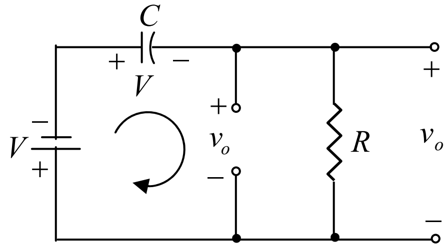


Figure 3.41: Determining v_o with the diode "off".

Applying Kirchhoff's voltage law around the input loop will result in

$$+V + V + v_o = 0 \text{ and } \quad v_o = -2V.$$

The negative sign resulting from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in figure 3.42 with the input signal. The output signal is clamped to $0\ V$ for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

For a clamping network:

The total swing of the output is equal to the total swing of the input signal.

This fact is an excellent checking tool for the result obtained.

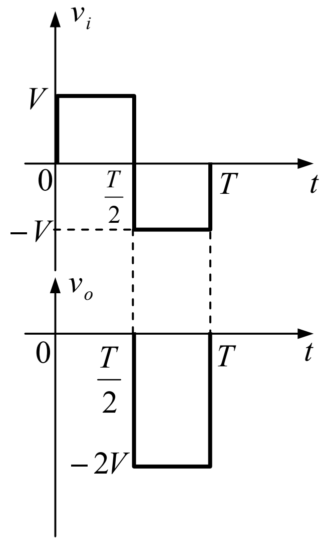


Figure 3.42: Sketching v_o.

In general, the following steps may be helpful when analyzing clamping networks:

1. Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.
2. During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.
3. Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage level.
4. Throughout the analysis maintain a continual awareness of the location and reference polarity for v_o to ensure that the proper levels for v_o are obtained.
5. Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.

Example: Determine v_o for the network of figure (a) for the input indicated.

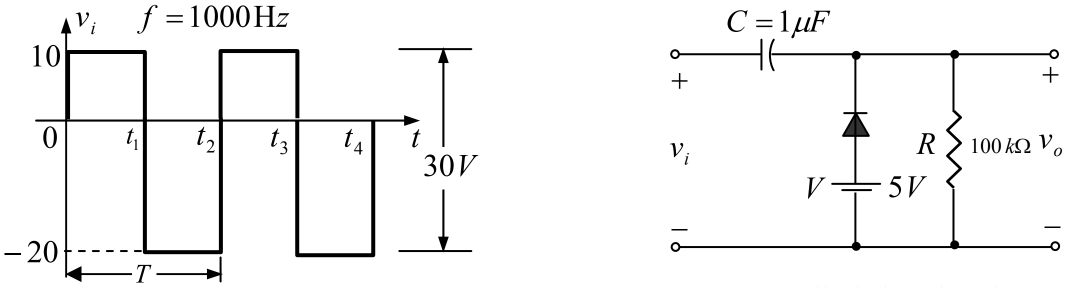


Figure (a): Applied signal and network.

Solution: Note that the frequency is 1000 *Hz*, resulting in a period of 1 *ms* and an interval of 0.5 *ms* between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in it short-circuit state as recommended by comment 1.

For this interval the network will appear as shown in figure (b). The output is across R, but it is also directly across the $5V$ battery if you follow the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5V$ for this interval.

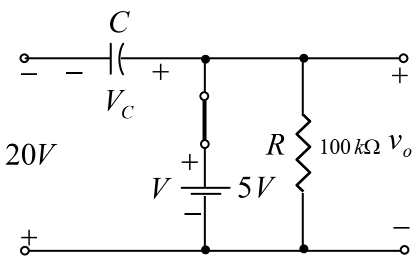


Figure (b): Determining v_o and V_C with the diode in the "on" state.

Applying Kirchhoff's voltage law around the input loop will result in

$$+20V - V_C + 5V = 0 \text{ and } V_C = 25\ V.$$

The capacitor will therefore, charge up to $25V$, as stated in comment 2. In this case the resistor R is not shorted out by the diode but a Thevenin's equivalent circuit of that portion of the network which includes the battery and the resistor will result in $R_{Th} = 0\,\Omega$ with $E_{Th} = \text{V} = 5\ V$.

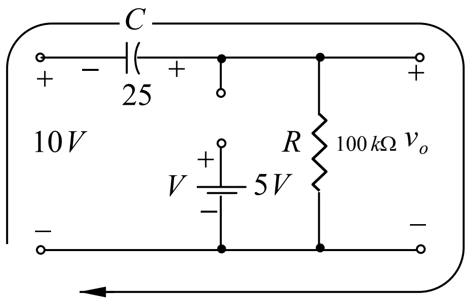


Figure (c): Determining v_o with the diode in the "off" state.

For the period $t_2 \rightarrow t_3$ the network will appear as shown in figure (c). The open-circuit equivalent for the diode will remove the $5V$ battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network will result in

$$-10\ V - 25\ V - v_o = 0 \text{ and } v_o = 35\ V.$$

The time constant of the discharging network of figure (c) is determined by the product RC and has the magnitude: $\tau = RC = (100\ k\Omega)\ (0.1\ \mu F) = 0.01\ \text{s} = 10\ ms$

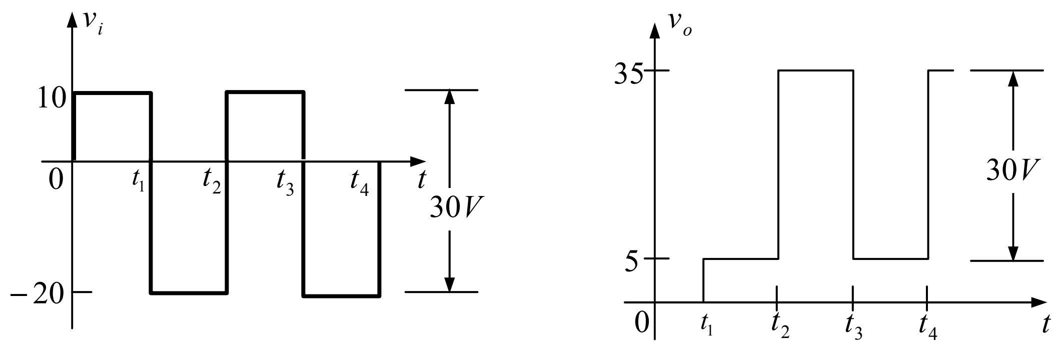


Figure (d): v_i and v_o for the clamper.

The total discharge time is therefore $5\tau = 5$ (10 ms) = 50 ms.
Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signals. The resulting output appears in figure (d) with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

Example: Repeat above example using a silicon diode with $V_\gamma = 0.7$ V.

Solution: For the short-circuit state the network now takes form of figure (a) and v_o can be determined by Kirchhoff's voltage law in the output section.

$$-5V + 0.7\ V + v_o = 0$$

and $v_o = 5V - 0.7\ V = 4.3\ V$

For the input section Kirchhoff's voltage law will result in

$$+20V - V_C - 0.7V + 5V = 0$$

and $V_C = 25\ V - 0.7\ V = 24.3\ V$.

For the period $t_2 \rightarrow t_3$ the network will now appear as in figure (b) with the only change being the voltage across the capacitor.

Applying Kirchhoff's voltage law yields

$$-10V - 24.3V + v_o = 0 \text{ and } v_o = 34.3\ V.$$

The resulting output appears in figure (c) verifying the statements that the input and output swings are the same.

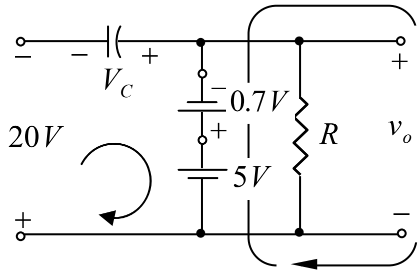


Figure (a): Determining v_o and V_C with the diode in the "on" state

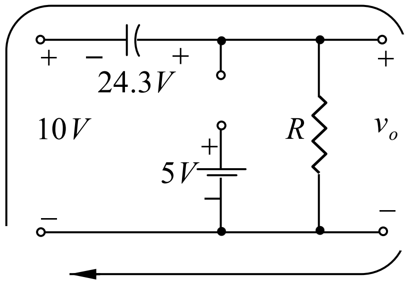


Figure (b): Determining v_o with the diode in the open state.

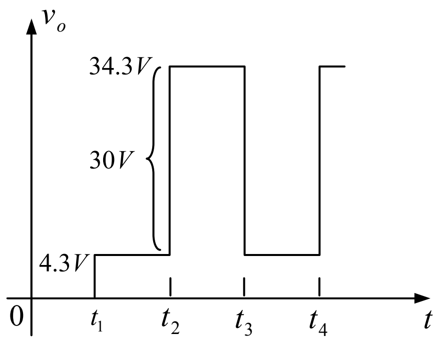
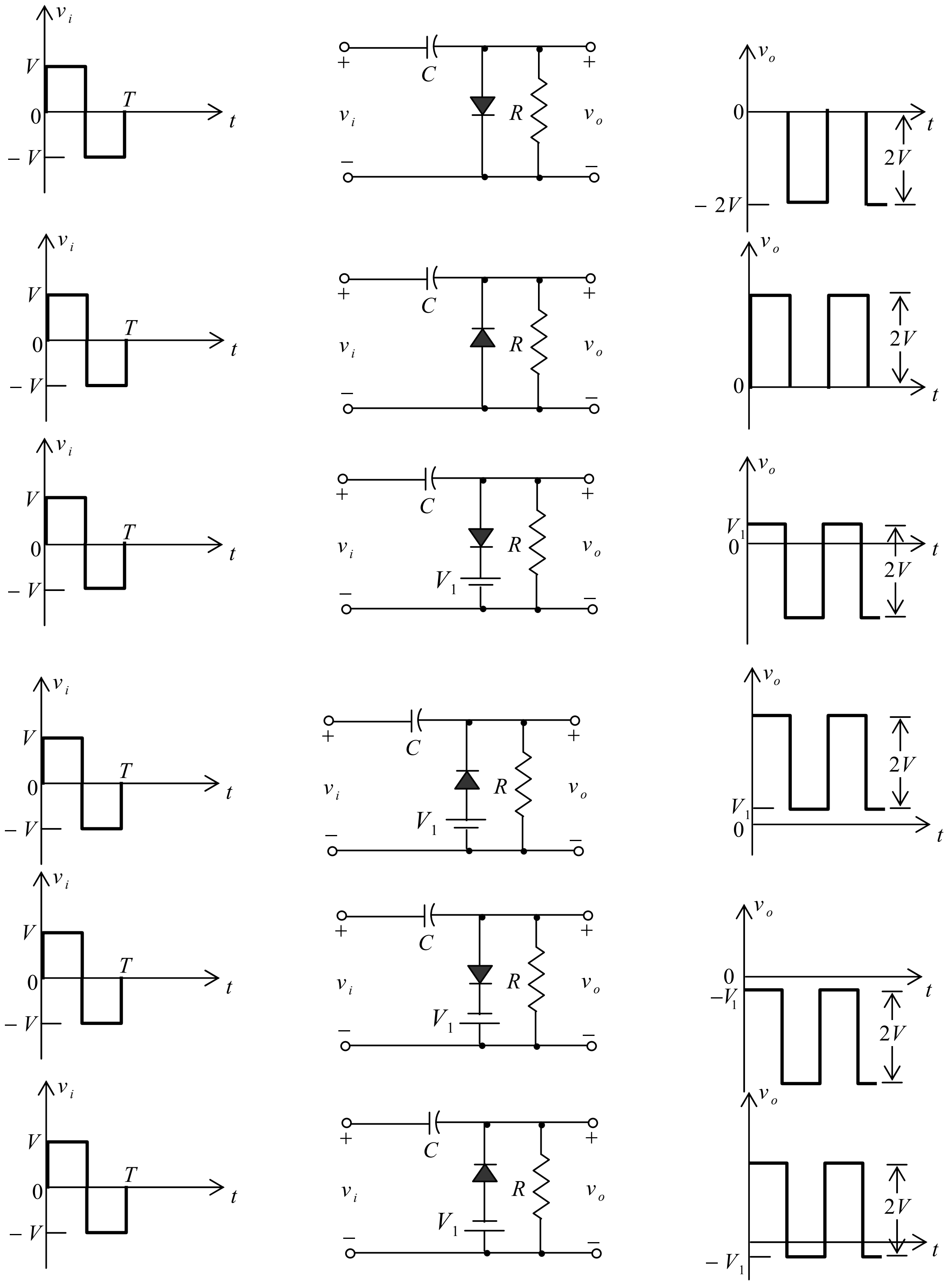


Figure (c): Sketching v_o.

SUMMARY CLAMPING NETWORKS



3.10 Zener Diode

The analysis of networks employing Zener diodes is quite similar to that applied to the analysis of semiconductor diodes. First the state of the diode must be determined followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. The Zener model to be employed for the "on" state and for the "off" state as defined by a voltage less than V_Z but greater than $0V$ with the polarity indicated as shown in figure 3.43.

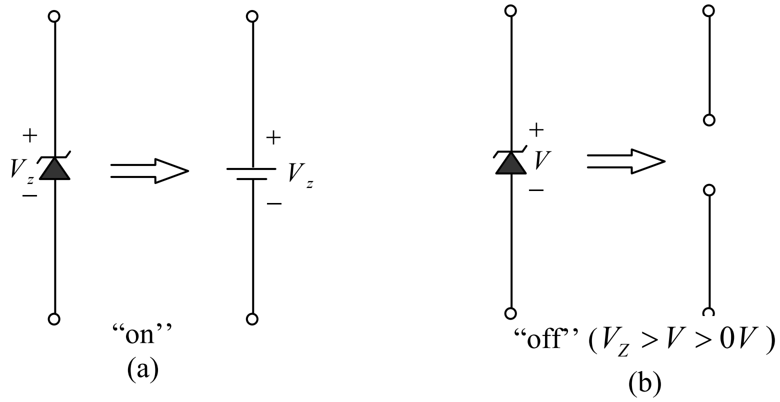


Figure 3.43: Zener diode equivalents for the (a) "on" and (b) "off" states.

3.10.1 Case-I (V_i and R_L fixed)

The simplest of Zener diode networks appears as shown in figure 3.44.

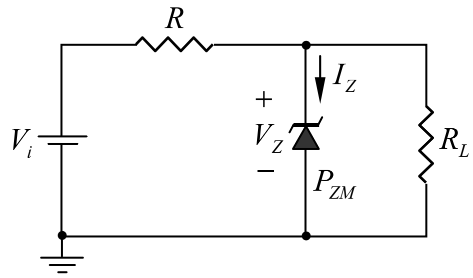


Figure 3.44: Basic Zener regulator.

The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. *Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.*

Open circuit voltage $V = V_L = \dfrac{R_L V_i}{R + R_L}$.

If $V \geq V_Z$, the Zener is "on" and if $V < V_Z$, the Zener is "off."

2. *Substitute the appropriate equivalent circuit and solve for the desired unknowns.*

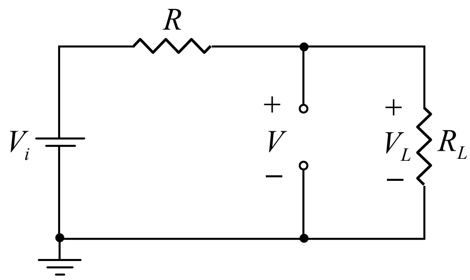


Figure 3.45: Determining the state of the Zener diode.

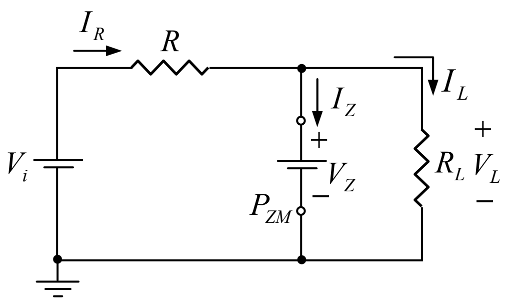


Figure 3.46: Substituting the Zener equivalent for the "on" situation.

When the Zener is "on" then $V_L = V_Z$ and $I_R = I_Z + I_L \Rightarrow I_Z = I_R - I_L$

where $I_L = \dfrac{V_L}{R_L}$ and $I_R = \dfrac{V_R}{R} = \dfrac{V_i - V_L}{R}$.

Power dissipated by the Zener diode $P_Z = V_Z I_Z \leq P_{ZM}$.

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Note:
If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on the Zener diode will turn "on" as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

Zener diodes are most frequently used in *regulator* network or a *reference* voltage. A simple regulator designed to maintain a fixed voltage across the load R_L. For values of applied voltage greater than required to turn the Zener diode "on," the voltage across the load will be maintained at V_Z volts. If the Zener diode is employed as a reference voltage, it will provide a level for comparison against other voltages.

Example: (a) For the Zener diode network of figure (a), determine V_L, V_R, I_Z and P_Z.

(b) Repeat part (a) with $R_L = 3k\Omega$.

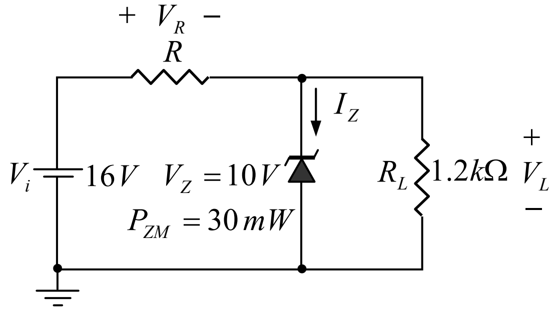


Figure (a)

Solution:
(a) Following the suggested procedure the network is redrawn as shown in figure (b).
Open circuit voltage

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2k\Omega(16\ \ V)}{1\ \ k\Omega + 1.2\ \ k\Omega} = 8.73\ \ V$$

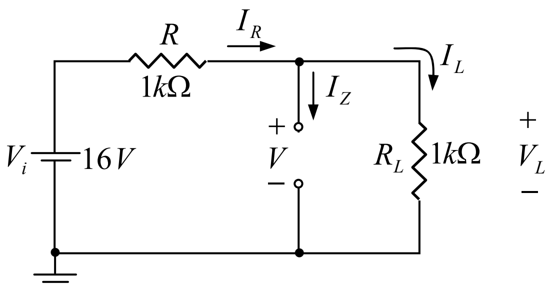


Figure (b): Determining V for the regulator of figure (a).

Since $V = 8.73\ V$ is less than $V_Z = 10\ V$ the diode is in the "off" state. Substituting the open-circuit equivalent we will find that
$V_L = V = 8.73\ V$, $V_R = V_i - V_L = 16\ V - 8.73\ V = 7.27\ V$
$I_Z = 0\ \ A$ and $P_Z = V_Z I_Z = 0\ W$.

(b) Open circuit voltage

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \ k\Omega(16\ \ V)}{1\ \ k\Omega + 3\ \ k\Omega} = 12\ \ V$$

Since $V = 12\ V$ is greater than $V_Z = 10\ V$, the diode is in the "on" state and the network of figure (c) will result.
$V_L = V_Z = 10\ V$ and $V_R = V_i - V_L = 6\ V$

with $I_L = \frac{V_L}{R_L} = \frac{10V}{3k\Omega} = 3.33\ \ mA$ and

$$I_R = \frac{V_R}{R} = \frac{6V}{1k\Omega} = 6\,mA.$$

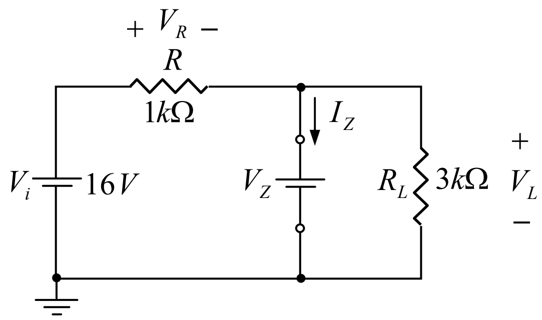


Figure (c): Network of figure (a) in the "on" state.

$I_Z = I_R - I_L = 6\ mA - 3.33\ mA = 2.67\ mA$. The power dissipated, $P_Z = V_Z I_Z = 26.7\ mW$ which is less than the specified $P_{ZM} = 30\ mW$.

3.10.2 Case-II (fixed V_i and variable R_L)

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) which will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z and the Zener device will be in the "off" state.

To determine the minimum load resistance that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$.

That is, $V_L = V_Z = \dfrac{R_L V_i}{R_L + R}$. Solving for R_L we have $R_{L_{\min}} = \dfrac{RV_Z}{V_i - V_Z}$.

Any load resistance value greater than the R_L obtained from above equation will ensure that the Zener diode is in the "on" sate and the diode can be replaced by its V_Z source equivalent.

This condition establishes the minimum R_L, but in turn specifies the maximum I_L as

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}}.$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z$$

and I_R remains fixed at $I_R = \dfrac{V_R}{R}$

The Zener current $I_Z = I_R - I_L$ resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value since I_R is constant.

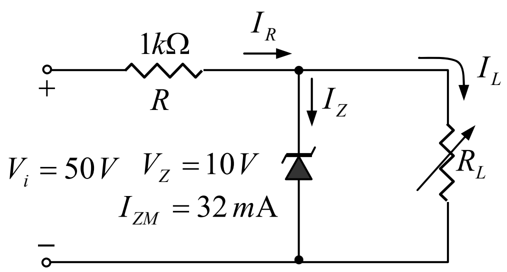
Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM}$$

and the maximum load resistance as $R_{L_{\max}} = \dfrac{V_Z}{I_{L_{\min}}}$.

Example: (a) For the network of figure shown determines the range of R_L and I_L that will result in V_{R_L} being maintained at 10 V.

(b) Determine the maximum voltage rating of the diode.



Solution:

(a) To determine the value of R_L that will turn the Zener diode on, apply equation

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\ k\Omega)(10V)}{50V - 10V} = \frac{10k\Omega}{40} = 250\Omega$$

The voltage across the resistor R is then determined by equation

$V_R = V_i - V_Z = 50\ V - 10\ V = 40\ V$ and $I_R = \dfrac{V_R}{R} = \dfrac{40\ \ V}{1\ \ k\Omega} = 40\ mA$.

The minimum level of I_L is then determined by equation

$$I_{L_{\min}} = I_R - I_{ZM} = 40\ mA - 32\ mA = 8\ mA$$

with $R_{L_{\max}} = \dfrac{V_Z}{I_{L_{\min}}} = \dfrac{10V}{8\,mA} = 1.25\,k\Omega$.

(b) $P_{\max} = V_Z I_{ZM} = (10\ V)(32\ mA) = 320\ mW$.

3.10.3 Case-III (fixed R_L and variable V_i)

For fixed values of R_L, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{\min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R} \text{ and } V_{i_{\min}} = \frac{(R_L + R)V_Z}{R_L}.$$

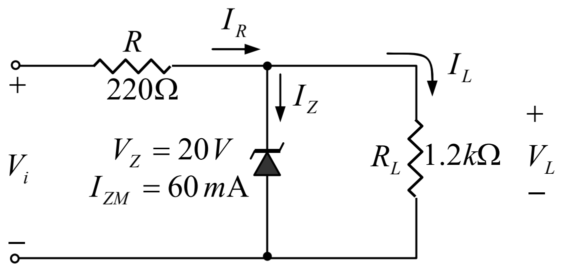
The maximum value of V_i is limited by the maximum Zener current I_{ZM}.

Since $I_{ZM} = I_R - I_L$, $\quad I_{R_{\max}} = I_{ZM} + I_L$

Since I_L is fixed at V_Z / R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{\max}} = V_{R_{\max}} + V_Z = I_{R_{\max}} R + V_Z .$$

Example: Determine the range of values of V_i that will maintain the Zener diode in the "on" state.



Solution:

$$V_{i_{\min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\,\Omega + 220\Omega + 20\,V)}{1200\,\Omega} = 23.67\,V$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\quad V}{1.2\quad k\Omega} = 16.67\ mA$$

$$I_{R_{\max}} = I_{ZM} + I_L = 60\quad m\text{A} + 16.67\quad m\text{A} = 76.67\ mA$$

$$V_{i_{\max}} = I_{R_{\max}} R + V_Z = (76.67\ mA)\ (0.22\ k\Omega) + 20\ V = 16.87\ V + 20\ V = 36.87\ V$$

3.10.4 Zener as a Reference Levels

Two or more reference levels can be established by placing Zener diodes in series as shown in figure 3.47. As long as V_i is greater than the sum of V_{Z_1} and V_{Z_2}, both diodes will be in the "on" state and the three reference voltages will be available.

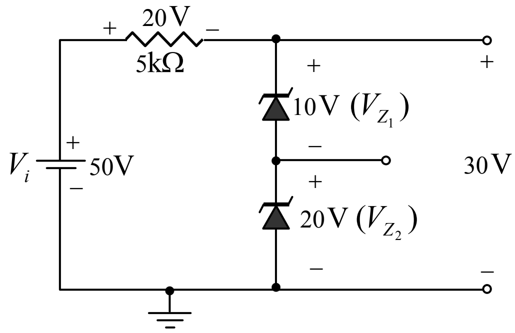


Figure 3.47: Establishing three reference voltage levels.

3.10.5 Zener as a Clipper

Two back-to-back Zener can also be used as an ac regulator as shown in figure 3.48. For the sinusoidal signal v_i the circuit will appear as shown in figure 3.49 at the instant $v_i = 10\ V$.

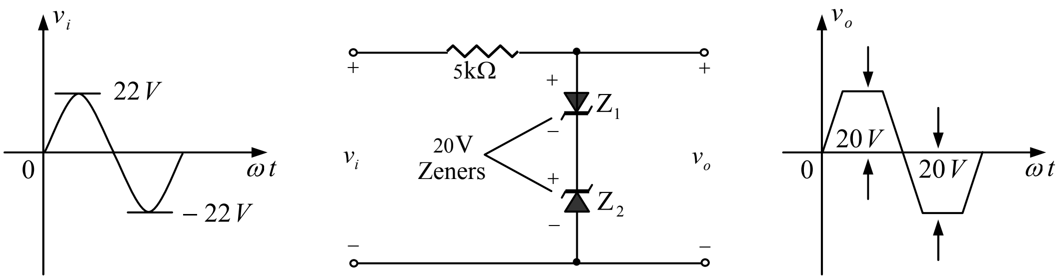


Figure 3.48: 40-V peak-to-peak sinusoidal ac regulator.

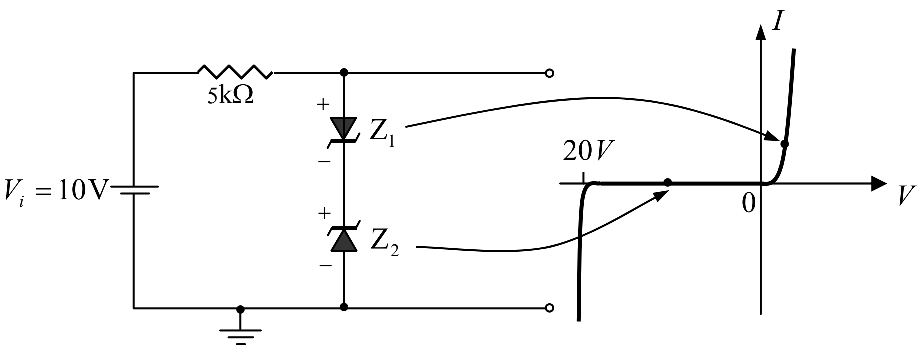


Figure 3.49: circuit operation at $v_i = 10\ V$.

The region of operation for each diode is indicated in the adjoining figure. Note that Z_1 is in a low-impedance region, while the impedance of Z_2 is quite large, corresponding with the open-circuit representation. The result is that $v_o = v_i$ when $v_i = 10\ V$.

The input and output will continue to duplicate each other until v_i reaches 20V. Z_2 will then "turn on" (as a Zener diode) while Z_1 will be in a region of conduction with a resistance level sufficiently small compared to the series $5k\Omega$ resistor to be considered a short circuit. The resulting output for the full range of v_i is provided in figure 3.48. Note that the waveform is not purely sinusoidal, but its rms value is lower than that associated with a full 22 V peak signal.